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Power Op Amp Protects Load Circuitry with Precise Current Limiting

by Tim Regan

Introduction

Snap, crackle and pop are the last sounds you ever want to hear when working with high power circuits, but such disturbing noises can be prevented by the new LT1970 op amp with variable current limiting.

Electronics designers do not often celebrate at the sound of components being overdriven to their demise. The resulting lingering scent of melted plastic and burnt metal can result in wasteful hours of discussion with curious co-workers who are interested in duplicating the explosive circuit. This cost in man-hours, added to the cost of the deceased components, can be staggering.

An important rule in working with high power circuitry is that any device that provides a significant amount of output power must provide some measure of protection of the circuitry it drives. Most power amplifiers only limit output current to the maximum current the amp can supply. This simple measure primarily protects the amplifier itself without much regard to the downstream load circuitry. Some power amplifiers provide slightly more protection with a programmable fixed current limit, where the maximum output current is fixed at a (hopefully) safer level using an external resistor. The LT1970 500mA power op amp takes load protection to the next logical step by providing an *on-the-fly* adjustable and precise output current limit that can continuously adapt to and protect load circuitry. The current limit, both sourcing and sinking, is adjusted through two 0V–5V voltage inputs, making it easy to create current limit control.

One obvious application of the LT1970 is in Automatic Test Equipment (ATE). In ATE, power amplifiers are used as pin drivers. These test pins force conditions at numerous points on a tested circuit board to determine both continuity and functionality. As each test point presents a unique load to the driver, the ability to tailor the voltage and maximum output current prevents damage to the board being tested. Without this flexibility, the tester itself could destroy the very unit it is testing should any test node present an unexpected load condition to the driver. ATE is only one obvious example. Myriad interesting applications are made

Snap, crackle and pop are the last sounds you ever want to hear when working with high power circuits, but such disturbing noises can be prevented by the new LT1970 op amp...

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Issue Highlights

Our cover article introduces the LT1970 power op amp, which provides on-the-fly adjustable and precise output current limit that can continuously adapt to and protect load circuitry. The current limit, both sourcing and sinking, is adjusted through two 0V–5V voltage inputs, making it easy to create current limit control.

The LT1970 is as easy to use as any basic op amp. It is a unity gain stable voltage feedback amplifier with good performance characteristics. The input offset voltage is less than 1mV, bias current is 160nA, gain bandwidth product is 3.6MHz and it slews at 1.6V/µs. It can operate with a total supply voltage of 36V over a –40°C to 125°C temperature range. It is also a power amplifier with a maximum output current limit of 800mA, both sourcing and sinking, built in thermal shutdown protection and comes in a small 20-pin TSSOP power package.

This issue also introduces two low noise op amps: the 1.9nV/√Hz LT6202 and the 0.95nV/√Hz LT6200. The LT6202 provides rail-to-rail input and output operation—meaning that maximum dynamic range can now be extracted on low supply voltages—with a supply current of only 2.5mA. The LT6200 offers even lower noise and distortion, and it includes a shutdown feature for standby conditions. These unity gain stable amplifiers are well suited to fast low noise applications because of their respective 100MHz and 165MHz gain bandwidth, low distortion, guaranteed noise specifications, and low offset voltage.

Also featured here is the LTC1921—the only fully integrated dual –48V supply and fuse monitor that meets common telecom specifications for supply range warning and can withstand the high transient voltages required by telecom systems. The LTC1921 achieves high accuracy, high reliability and ease of use by combining an accurate internal reference, precision comparators and trimmed resistor networks in one package. Few external components are required, and none affect the threshold accuracy.

Our power articles include a feature about the Powered Ethernet. This is the first of a three part series, covering the power details of the system, with a particular focus on the PSE and its characteristics. Part 2 will cover the PD in detail, while Part 3 will discuss the nuances of detection and classification—the mechanism that the 802.3af standard uses to ensure that PDs receive power while legacy data-only devices remain unpowered.

Another feature power article introduces the LT3430—a monolithic step down DC/DC converter that features a 3A peak switch current limit and the ability to operate with up to 60V input. The LT3430 runs at a fixed frequency of 200kHz and is packaged in a small thermally enhanced 16-pin TSSOP package to save space and simplify thermal management. The 5.5V to 60V input range makes the LT3430 ideal for FireWire® Peripherals (typically 8V to 40V input), as well as automotive systems requiring 12V, 24V and 42V input voltages (with the ability to survive load dump transients as high as 60V). It is designed to maintain excellent efficiencies at both high and low input-to-output voltage differentials over a wide input voltage range.

Starting on page 20 are ten new Design Ideas covering a variety of applications, from a simple way to reduce output ripple in a positive voltage to negative voltage DC/DC converter to using a single ADC to simultaneously digitize two signals. See page 20 for a complete list of the Design Idea articles.

At the back are five New Device Cameos. See www.linear.com for complete device specifications and more applications information.

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For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

LTC in the News...

On July 23, Linear Technology Corporation announced its financial results for the 4th quarter and fiscal year 2002. According to Robert H. Swanson, Chairman of the Board and CEO, "Fiscal 2002 was a tough year, however, even in a difficult environment the Company was highly profitable and cash flow was positive. The quarter just ended was our strongest quarter within the year as sales and profits grew 8% and 7% respectively over the March quarter. Operating income grew 10% sequentially and our return on sales was 39% for the quarter.

Although we have seen improvements across end markets in the last two quarters, our backlog, while improving, is still low. General business conditions continue to be tenuous and visibility remains low as customers order only to supply immediate demand. Therefore, confidently and accurately forecasting future financial results remains difficult. We are well positioned in some new programs at customers, which could ramp up late in the September quarter and in the following quarter. The summer, or September quarter, is historically our slowest and in the current business environment, we expect that to be true this year also. Consequently, we estimate that sales and profits will remain similar to the June quarter with growth resuming in the December quarter."

The Company reported net sales of $512,282,000 and net income of $197,629,000 for the year ended June 30, 2002. Diluted earnings were $0.60 per share.

LT1970, continued from page 1

possible by the full and immediate control of a power amplifier output voltage and current.

A Look Inside the LT1970

The LT1970 is as easy to use as any basic op amp. It is a unity gain stable voltage feedback amplifier with good performance characteristics. The input offset voltage is less than 1mV, bias current is 160nA, gain bandwidth product is 3.6MHz and it slews at 1.6V/µs. It can operate with a total supply voltage of 36V over a –40°C to 125°C temperature range. It is also a power amplifier with a maximum output current limit of 800mA, both sourcing and sinking, built in thermal shutdown protection and comes in a small 20-pin TSSOP power package. The underside of the package has an exposed metal pad to facilitate heat sinking. These are only the basic amplifier characteristics; there are other built-in features that set the LT1970 apart.

Figure 1 is a block diagram of the LT1970. A standard amplifier topology is composed of a differential-input transconductance stage, g_{m1}, driving a unity gain high current output stage. The inputs can handle 36 volts differentially without conducting any current. This is an important feature when the current limit amplifiers become active and take control of the output voltage.

The current limit amplifiers, labeled I_{SINK} and I_{SRC}, provide the unique output current limiting control in both the sinking and sourcing direction. These amplifiers connect to the high impedance output of the input stage and have a much higher transconductance than the g_{m1} stage. The current limit amplifiers monitor the voltage between two sense input pins, $SENSE^+$ and $SENSE^-$ (for simplicity this voltage difference will be referred to a simply V_{SENSE}). These input pins are typically connected across a small external current sensing resistor, R_{CS}. As shown each amplifier has an independently controlled offset voltage, V_{SNK} and V_{SRC}, which set the thresholds for the output current limit. When V_{SENSE} is less than either offset voltage, the current limit amplifiers are disconnected from the signal path. This functionality is indicated by diodes D1 and D2.

When V_{SENSE} exceeds either current limit offset voltage the applicable current limit amplifier becomes active and takes control of the signal path from the input stage, g_{m1}. Feedback control of the amplifier is now through the current limit path and the output current is regulated to a value of V_{SENSE}/R_{CS} with V_{SENSE} forced to the value of the threshold voltage, V_{SNK} or V_{SRC} depending on the direction of the output current flow. Voltage control of these thresholds is the key to on-the-fly current limit adjustments.

Two current limit control inputs, V_{CSNK} and V_{CSRC} set the current limit thresholds. These pins take a 0V to 5V input to independently control the maximum sinking or sourcing current. The sinking current limit threshold, V_{SNK}, is equal to one tenth the voltage applied to the V_{CSNK} pin (likewise for the sourcing current limit). This sets the maximum output current in either direction to a voltage-controlled value of:

$$I_{OUT(MAX)} = \frac{V_{CSNK} \text{ or } V_{CSRC}}{10 \bullet R_{CS}}$$

If R_{CS} is selected to be a 1Ω resistor, a 0V to 5V control voltage adjusts the current limit over the range of 4mA to 500mA. The accuracy of the current limit at 500mA is guaranteed to be 2% maximum or within 10mA. The lower limit of 4mA, instead of 0mA, is intentional. A non-linearity with control input voltages less than 0.1V is built-in to prevent the sourcing and sinking limit amplifiers from ever being activated at the same time. This would

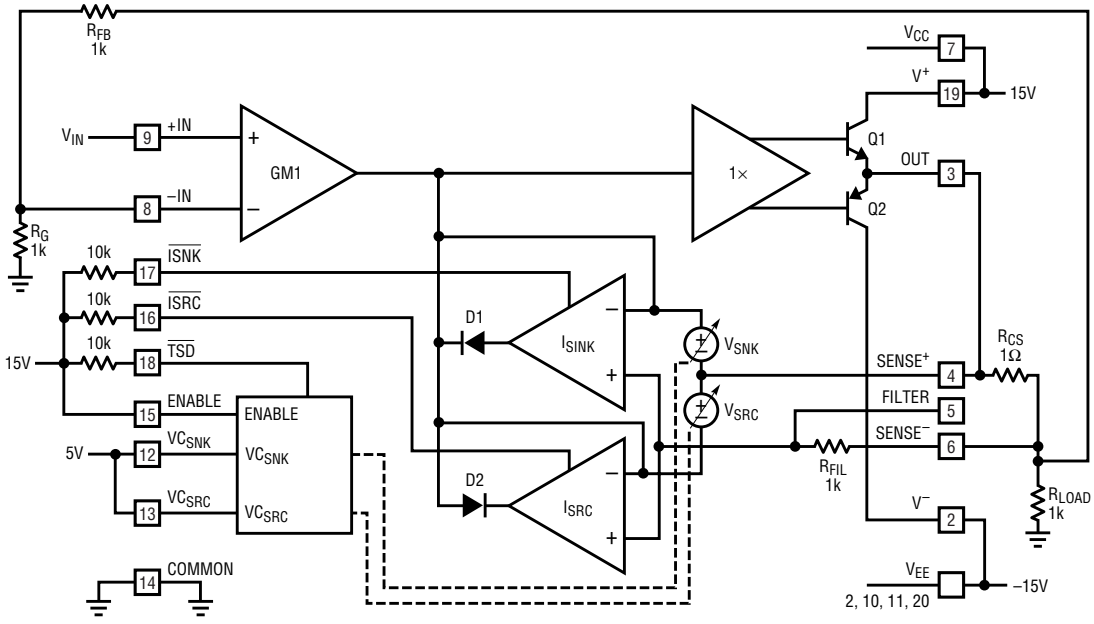


Figure 1. The LT1970 is a basic power amplifier with built-in voltage control of the output current limit.

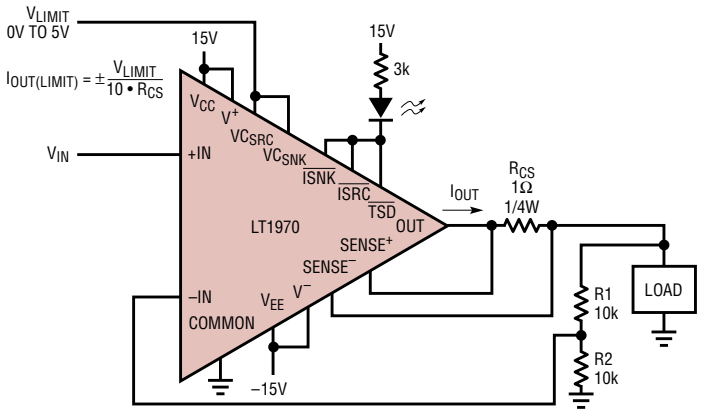


Figure 2. A typical LT1970 circuit

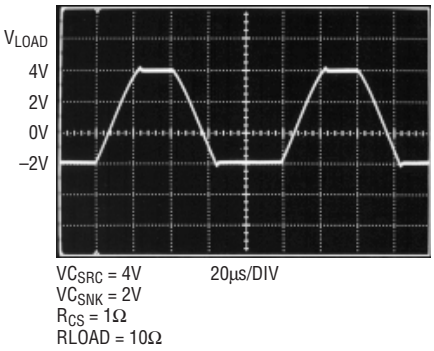


Figure 3. Current limiting clamps the output voltage of the circuit of Figure 2 at precise levels. Independent control allows different sourcing and sinking current limits.

result in an uncontrolled output. The bandwidth from the control inputs to the output is 2MHz, which can be useful for AC current modulation. The response time for the current limit amplifiers to take control of the output is fast, typically 4µs.

Other features include an active high enable input, three open collector error flags and separate power supply input lines. The enable input turns off the LT1970 and drops the supply current to 600µA. It also places the output stage into a high impedance, zero output current, state. The error flags, which can drive LEDs, indicate that the driver is in current limit, in either direction, or that a load condition has caused the LT1970 to enter its thermal shutdown protection. The V_{CC} and V_{EE} supply pins power all of the internal circuitry except for the high current output stage. The output stage is powered from the V^+ and V^- pins, which conduct all of the output current. Biasing the output stage from lower supply voltage levels can significantly reduce the power dissipation in the output stage in high current applications.

Application Ideas Abound

Having complete control over the voltage and current applied to a load in a single device leads to innumerable application possibilities. The ease of limiting or modulating the output current of the LT1970 solves many circuit problems and can protect many a load circuit. Here are a few ideas.

Figure 2 shows the basic application of the LT1970 power amplifier. This is a simple noninverting gain of two amplifier until the current limiting is activated. Figure 3 shows the separate current limiting control for sourcing and sinking. With V_{CSRC} set to 4V, a sense resistor R_{CS} of 1Ω and a 10Ω load on the amplifier, the maximum output voltage is 4V due to current limiting at 400mA. Setting V_{CSNK} to 2V sets the sinking current in this example to 200mA. The three error flags are ORed together to provide a single indication of the LT1970 reaching current or thermal limits.

Need More than 500mA?

The 500mA output stage of the LT1970 is adequate for many applications, but there are also some higher current applications that can benefit from the unique current limit control. Figure 4 shows how easy it is to boost the output current to ±5A using an external complementary pair of MOSFETs. The output current sense resistor is

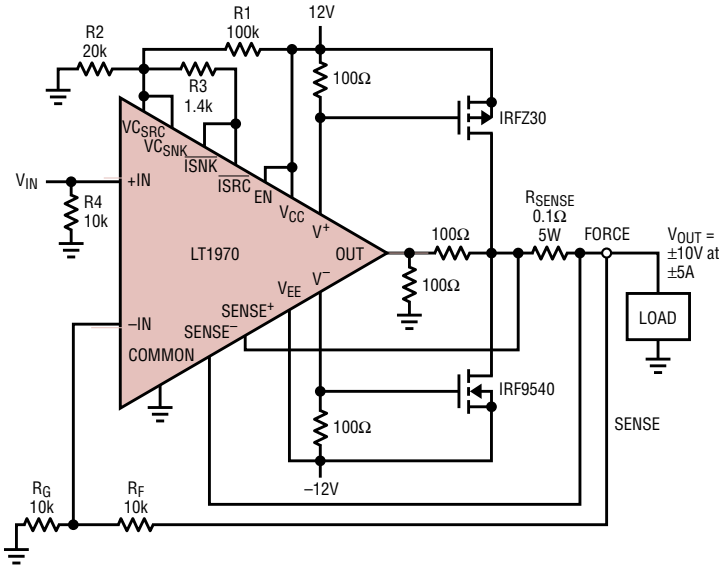


Figure 4. Boosting the output current capability to ±5A

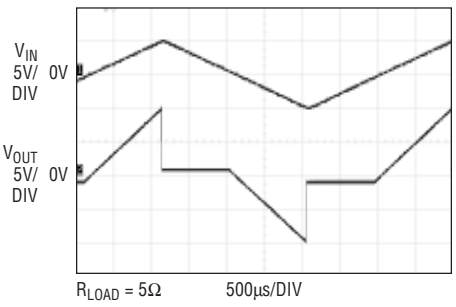


Figure 5. Snap-back current limiting provides an added measure of safety.

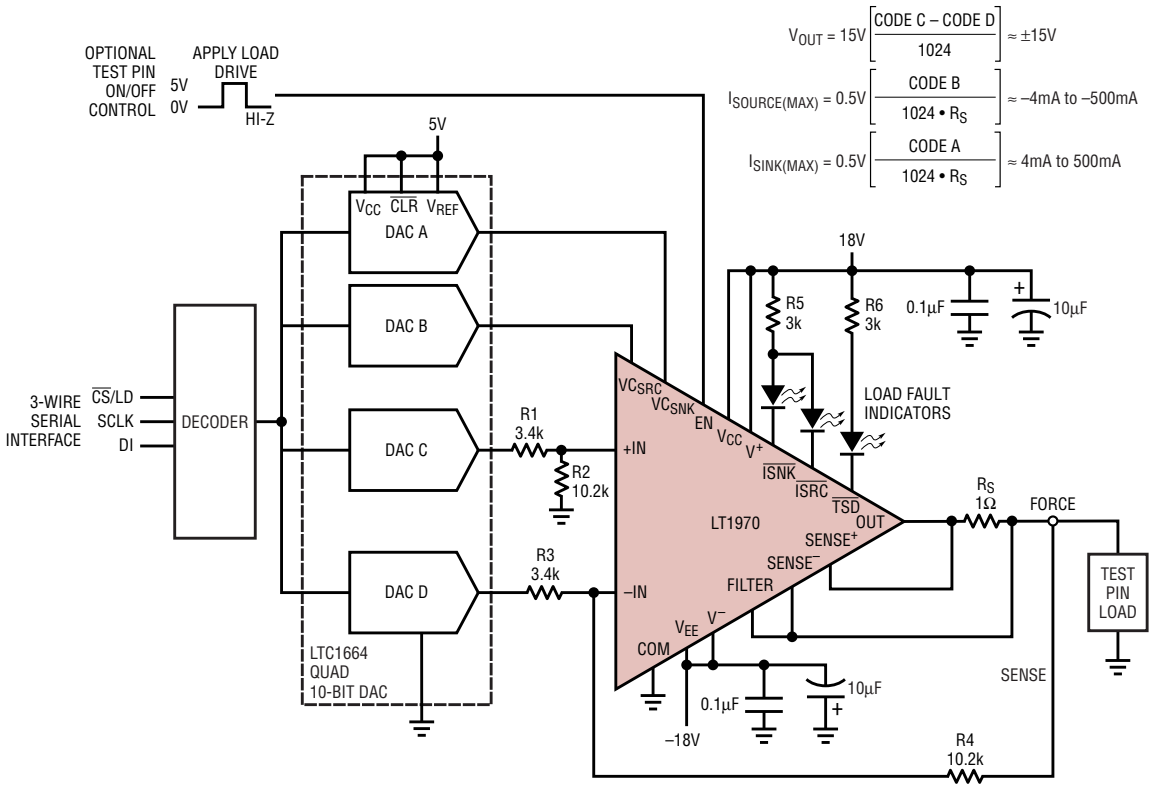


Figure 6. An analog pin driver with DAC controlled parameters

scaled down to 0.1Ω to extend the same 0V to 5V current limit control to a range from 40mA to 5A. The gate voltage drive is developed from the V^+ and V^- supply pins with the current needed by the LT1970 output stage as it drives a 100Ω load. This Class B power stage is intended for DC and low frequency, <1kHz, designs as crossover distortion between sourcing and sinking current becomes evident at higher frequencies. In very high current designs, having externally connected gain-setting resistors allows for Kelvin sensing at the load. By connecting the feedback resistor right at the load, the voltage placed on the load is exactly what it should be. Any voltage drop across the current sense resistor is inside the feedback loop and thus does not create a voltage error.

"Snap-Back" Current Limiting

Figure 4 also shows a unique way to use the open-collector error flags to provide extra protection to the load circuitry. When the amplifier enters current limit in either direction, the appropriate error flag goes low. This high impedance to 0V transition can provide a large amount of hysteresis to the current limit control inputs, forcing a drastic reduction in output current. Resistors R1, R2 and R3 in this example set the current limit control at 2V max and 200mV min. Should the load current ever exceed the predetermined maximum limit, the output current snaps back to the min level. The output current remains at this lower level until the signal drops to a point where the load current is less than the minimum set value. When the signal is low enough, the flag output goes open and the current limit reverts to the maximum value. This action simulates an automatically resetting fuse. Figure 5 shows the action of this hysteresis with a maximum current limit of 2A snapping back to 200mA when exceeded in either direction.

Digitally Controlled V and I

Figure 6 shows a way to combine a D-to-A converter such as the quad 10-bit LTC1664 with an LT1970 to give complete control over output voltage and current. This circuit could be applied as an analog pin driver for ATE applications. The circuit is a difference amplifier with a gain of three to produce ±15V output from 0V to 5V DAC generated inputs. The two other DACs control the maximum output current. Again, Kelvin sensing at the load pin preserves precision voltage control across the load. The enable pin of the LT1970 can be used to strobe new voltage and current limit settings to the load after each DAC update.

Power Comparator

The simple circuit shown in Figure 7 is a different type of comparator. This comparator steers the direction of current flow through the load, which could be resistive, capacitive or inductive. The magnitude of the current is controlled by the normal current limit control input voltages and can be DC or modulated up to 2MHz. There is no voltage feedback so the input voltage drives either the top or the bottom output transistor fully on. The output will source or sink the load current depending on the polarity of the input voltage. On a cautionary note, if the load cannot

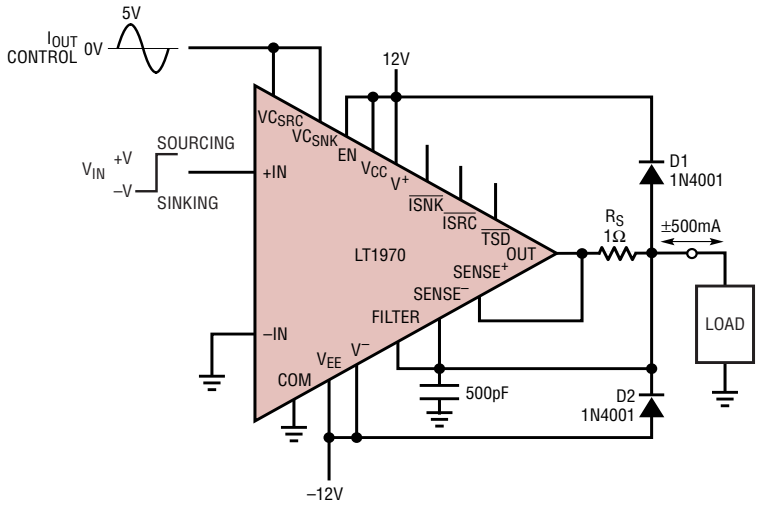


Figure 7. A power comparator steers a controlled amount of output current.

conduct the controlled current level the output voltage will go to one supply rail or the other. Clamp diodes from the output to the supplies are shown together with a small frequency compensation capacitor at the SENSE$^-$ pin. This is for the case where the load is highly inductive and able to generate high voltage transients at the moment of current reversal.

Symmetrical Voltage Clamp

Voltage clamping amplifier circuits are often complicated designs requiring back to back diodes, Zeners or references to limit the output swing to a precise level. The ability to linearly vary the clamped voltage just adds more to the challenge. A symmetrical clamp circuit (Figure 8) is fairly simple to implement by using the current limit sense amplifiers of the LT1970 to monitor just the output voltage, instead of the output current. The amplifier operates normally until the V_{SENSE+} voltage exceeds the threshold controlled by the current limit control input voltages. The internal divide by 10 from the control input to the clamping threshold requires an external divide by 20 resistor network between the circuit output and the SENSE$^+$ pin. This allows a 0V to 5V control signal to produce an output clamp voltage over the range of ±80mV to ±10V. Since the threshold voltages are the same in either direction the output clamping is symmetrical. Figure 9 illustrates this clamping action.

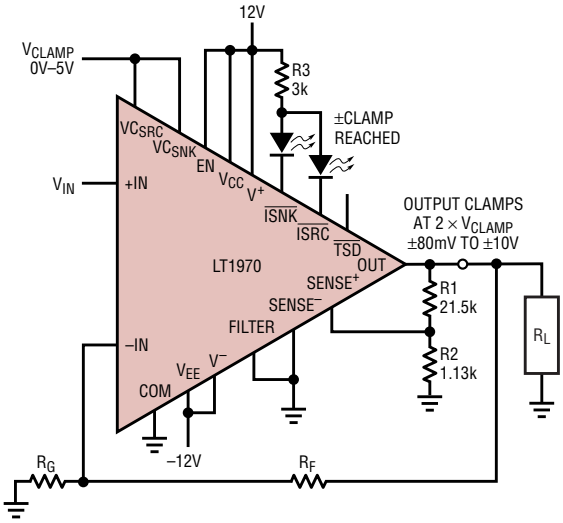


Figure 8. Symmetrical output voltage clamping is easy to implement with the LT1970.

Conclusion

The LT1970 is a versatile and easy to use power op amp with a built-in precision adjustable current limit, which can protect load circuitry from damage caused by excessive power from the amplifier. This feature is particularly useful in ATE systems where the load is variable (and possibly faulty) at each tested node. Tight control of the output current in these systems is important to prevent damage to the tested unit. The LT1970's ability to control both output voltage and current makes possible many innovative applications that otherwise would be difficult or impracticle to implement.

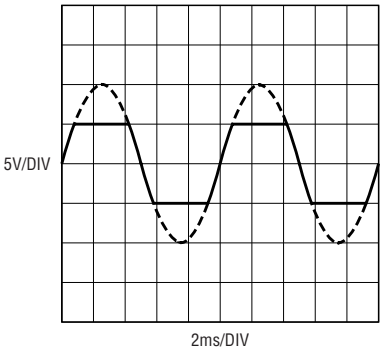


Figure 9. Voltage clamping response of the circuit of Figure 8

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

60V/3A Step-Down DC/DC Converter Maintains High Efficiency over a Wide Range of Input Voltages

by Mark W. Marosek

Introduction

The LT3430 is a monolithic step-down DC/DC converter that features a 3A peak switch current limit and the ability to operate with up to 60V input. The LT3430 runs at a fixed frequency of 200kHz and is packaged in a small thermally enhanced 16-pin TSSOP package to save space and simplify thermal management. The 5.5V to 60V input range makes the LT3430 ideal for FireWire® Peripherals (typically 8V to 40V input), as well as automotive systems requiring 12V, 24V and 42V input voltages (with the ability to survive load dump transients as high as 60V). It is designed to maintain excellent efficiencies at both high and low input-to-output voltage differentials over a wide input voltage range. Its current mode architecture adds flexible frequency compensation with no restriction on the use of a ceramic output capacitor—resulting in small solutions with extremely low output ripple voltage.

The LT3430 is pin compatible with the LT1766 (60V, 1.5A, 200kHz) and LT1956 (60V transient, 1.5A, 500kHz) step down DC/DC converters.[1]

LT3430 Features

- ❏ Wide input range 5.5V to 60V
- ❏ 3A peak switch current
- ❏ Small thermally enhanced 16-pin TSSOP Package
- ❏ Constant 200kHz switching frequency
- ❏ 100mΩ saturating switch
- ❏ Current mode architecture
- ❏ Peak switch current maintained over full duty cycle range
- ❏ 30µA shutdown current
- ❏ 1.2V feedback reference
- ❏ Easily synchronizable

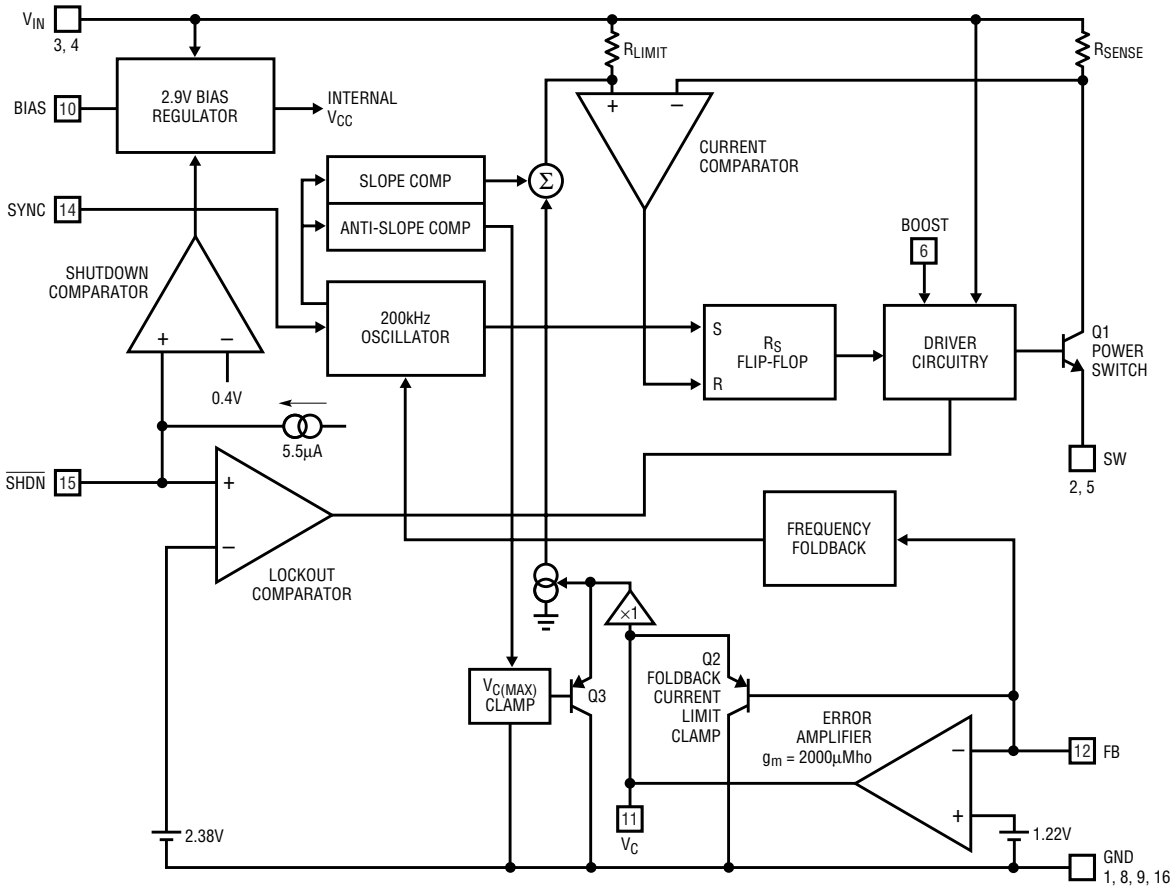
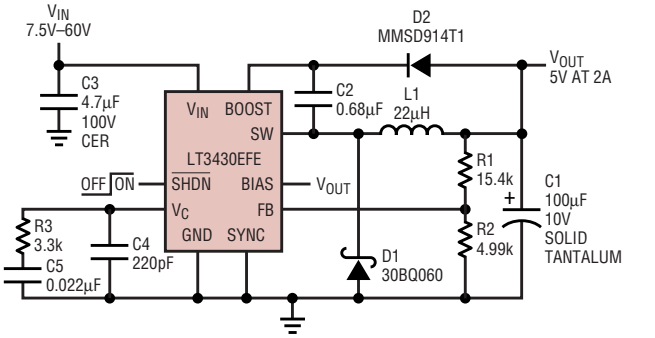


Figure 1. Simplified block diagram



C1: AVX D CASE 100µF 10V TPSD107M010R0100 (207) 282-5111
C2: AVX 0.68µF X7R 16V 0805YC684KAT1A
C3: UNITED CHEMI-CON 4.7µF 100V TCCR70E2A475M (847) 696-2000
C4: AVX 220pF X7R 50V 08055A221KAT
C5: AVX .022µF X7R 16V 0805YC223KAT
D1: INTERNATIONAL RECTIFIER 60V 3A SCHOTTKY 30BQ060 (310) 322-3331
L1: SUMIDA 22µH CDRH104R (847) 956-0667

Figure 2. Efficient 42V to 5V step-down converter

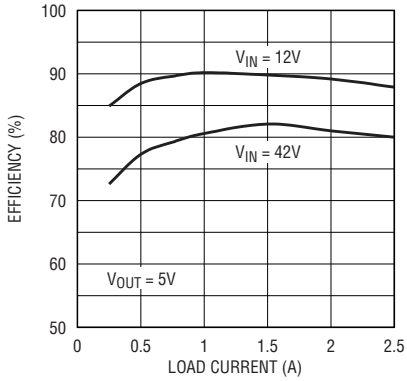


Figure 3. Efficiency of the circuit shown in Figure 2

Circuit Description

The block diagram in Figure 1 shows all of the key functions of the LT3430 step-down DC/DC converter. Its current mode architecture uses two feedback loops to control the duty cycle of the internal power switch—a transconductance error amplifier monitors the error between output voltage (via the FB pin) and an internal 1.22V reference, and a current sense comparator monitors switch current on a cycle-by-cycle basis. The LT3430 runs at a fixed frequency of 200kHz or can be externally synchronized up to 700kHz using the SYNC pin. The LT3430 includes a shutdown pin with an accurate 2.38V threshold for undervoltage lockout, and a 0.4V threshold for micropower shutdown (I_Q = 30µA). The BIAS pin provides power savings by allowing control circuitry to be supplied from the output. The LT3430 also uses frequency foldback and current limit foldback to control power dissipation in the IC, external catch diode and inductor in the event of an output short circuit to ground.

Peak Switch Current over the Full Duty Cycle Range (Not Your Average Current Mode Converter)

The LT3430 maintains peak switch current over the full duty cycle range (wide input voltage range). Although the LT3430 uses a current mode architecture—to allow small, low noise power supply solutions—its peak switch current does not fall off at high duty cycles, unlike most current mode converters. This typical reduction of peak switch current is a result of the necessary slope compensation in the current sensing loop, which exists to prevent sub-harmonic oscillations for duty cycles above 50%. The LT3430 uses a patented process to cancel the effect of slope compensation on peak switch current without affecting frequency compensation. For applications that require high duty cycles, this offers significant advantages—including a lower inductor value, lower minimum V_{IN} and/or higher output current capability—over typical current mode converters with similar peak switch current limits.

Efficiency

The LT3430 is designed to provide efficient solutions at both high and low input-to-output voltage differentials, over a wide input voltage range. A typical high input voltage application with a large input-to-output differential, a 42V to 5V converter, is shown in Figure 2. To obtain high efficiency at high input voltages requires fast output-switch edge rates, and minimal quiescent current drawn from the input at light loads. The BIAS pin allows power for the internal control circuitry to be supplied from the regulated output if it is greater than 3V. The peak efficiency for a 42V to 5V conversion is greater than 82% as shown in Figure 3.

The LT3430 is also capable of excellent efficiencies at lower input voltages. The peak efficiency for a 12V to 5V converter is greater than 90% as is also shown in Figure 3. One important factor in achieving high efficiency for low input-to-output voltage conversions is to use a low resistance saturating switch. A prebiased capacitor, connected between the BOOST and SW pins, generates a boost voltage above the input supply during switching. Driving the switch from this boost voltage allows the 100mΩ power switch to fully saturate. Any output voltage of at least 3.3V is enough to generate the required boost supply.

Space Saving and Low Output Ripple Voltage Solutions

The high switching frequency and current mode architecture of the LT3430 combine to make it possible to design space-saving solutions with low output ripple voltage. The 200kHz switching frequency of the LT3430 reduces the inductor value required to achieve low inductor ripple current, allowing for the use of a physically smaller inductor. The current mode architecture of the LT3430 allows for flexible frequency compensation to accommodate various output voltages, load currents and output capacitor types. This flexibility allows for a small, low ESR ceramic capacitor to be used at the output—making for an extremely low output ripple voltage solution in a small space.

continued on page 19

New Power for Ethernet—The LTC4255 Delivers (Part 1 of a 3-Part Series)

by Dave Dwelley

Introduction

For years, data has passed over Ethernet CAT-5 networks, primarily to and from servers and workstations. The IEEE 802.3 group, the originator of the Ethernet standard, is currently at work on an extension to the standard, known as 802.3af, which will allow DC power to be delivered simultaneously over the same wires.[1] This promises a whole new class of Ethernet devices, including link-powered IP telephones, wireless access points, and PDA charging stations, which do not require additional AC wiring or external power transformers ("wall warts"). With about 13W of power available, small data devices can be powered by their Ethernet connection, free from AC wall outlets.

Modern Ethernet networks and traditional telephone systems share much in common. Both typically send data or voice over unshielded twisted-pair connections, and both are typically connected in a "star" configuration, where each terminal is connected to a central switch or hub. One significant difference, however, is that traditional phones are usually powered through the same wire as their "data" connection, whereas Ethernet devices require a local source of power. 802.3af changes this, by allowing the central switch to provide 48VDC at up to 13W through the familiar RJ45 connector. Sophisticated detection and power monitoring techniques prevent damage to legacy data-only devices, while still supplying power to newer, Ethernet powered devices over the CAT-5 wire.

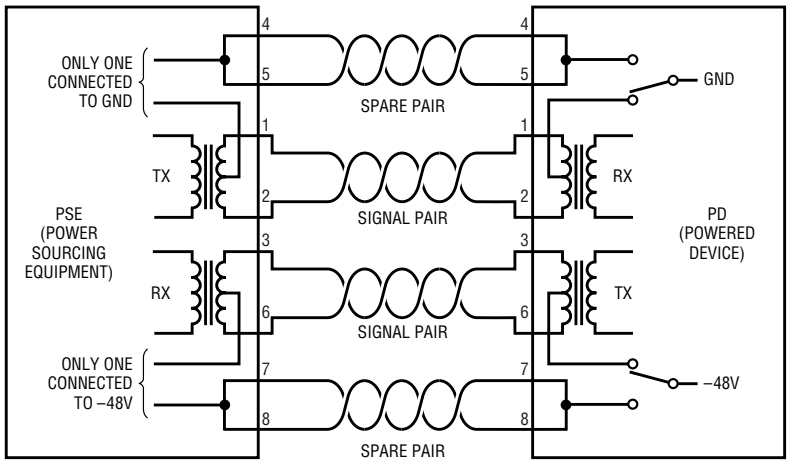


Figure 1. Delivering power over existing Ethernet cables using the center tap of the transformer

A device that supplies power is called a PSE (for Power Sourcing Equipment); a device that draws power from the wire is called a PD (for Powered Device). A PSE is typically an Ethernet switch, router, hub, or other network switching equipment that is commonly found in wiring closets or under desks where CAT-5 cables converge. PDs can take many forms: digital IP telephones, wireless network access points, PDA or notebook computer docking stations, cell phone chargers, and HVAC thermostats are examples of devices that can draw their power from the network. Virtually any device that requires a data connection and can run from 13W or less can shed its AC power cord or batteries and operate off the RJ45 connector alone.

This article is the first in a three-part series on Powered Ethernet. This issue features Part 1, which covers the power details of the system, with a particular focus on the PSE and its characteristics. Part 2 will cover the PD in detail, while Part 3 will discuss the nuances of detection and classification—the mechanism that the 802.3af standard uses to ensure that PDs receive power while legacy data-only devices remain unpowered.

Power Over Ethernet Glossary

- ❑ **PSE (Power Sourcing Equipment)**—usually a router or hub, but can also be a midspan
- ❑ **PD (Powered Device)**—any device that is powered over the Ethernet by a PSE: can be a phone, a WAP (Wireless Access Point) or even a PDA charger or an exit sign
- ❑ **Midspan**—a device that plugs in-line to convert a conventional router to a PSE; typically powers the spare pairs
- ❑ **Signal Pairs**—pairs 1-2 and 3-6 in CAT-5 cable
- ❑ **Signal Pairs**—pairs 4-5 and 7-8 in CAT-5 cable
- ❑ **PHY (Physical Layer Interface)**—the differential transceiver that transmits and receives data over the link

Delivering Power over Ethernet Cables

A CAT-5 Ethernet cable contains four unshielded twisted pairs of 24-gauge copper wire in a common sheath, with RJ45 connectors on each end. In a typical 10BASE-T or 100BASE-TX

(10/100) network, two of the pairs (the "signal pairs") are used for data transmission (one for transmit, one for receive) and two pairs (the "spare pairs") are unused. 1000BASE-T (Gigabit over Copper) networks use all four pairs, and are compatible with most aspects of Powered Ethernet, although there are some incompatibilities and some aspects of the 802.3af standard do not explicitly support 1000BASE-T.

A PSE is required to provide a nominal 48V DC between either the signal pairs or the spare pairs (but not both)—see Figure 1. The power is applied as a common mode voltage difference between the two powered pairs, typically by powering the center-taps of the isolation transformers used to couple the differential data signals to the wire. Since Ethernet data lines are transformer-isolated at each end of the wire, this 48V potential difference between the transmit pair and the receive pair has no effect on the data transceivers on either end. The spare pairs can be tied together and powered directly (as shown in Figure 1), or they can be powered via transformer center taps in the same manner as the signal pairs if compatibility with 1000BASE-T is required.

The 48V supply used to power the line must be isolated from the PSE chassis ground to maintain the isolated link between the PSE and the PD. The IEEE defines two methods of isolation, named Environment A and Environment B. Environment A PSEs must isolate the 48V supply from the PSE chassis but need not isolate between adjacent ports, while the more stringent Environment B requires that ports be isolated both from the chassis and each other. In keeping with telecom conventions, the 48VDC supply is often referred to as a –48V supply; however, since the supply must be isolated from the chassis, which end is deemed to be "ground" is relatively arbitrary.

PSEs are physically located in one of two places: either integrated into data switch/router/hub devices, or as a standalone unit known as a "midspan" that connects in-line between an existing data switch and the PD. An integrated PSE/switch is allowed to drive either set of pairs, but typically will drive the signal pairs. A midspan is required to drive the spare pairs.

PSE Power Requirements

- ❑ Output is –44V to –57V (usually –48V), isolated from chassis—
  Environment A: ports not isolated from each other
  Environment B: isolated from chassis and port-to-port
- ❑ 15.4W (44V • 350mA) minimum power supply—current limit may drop as voltage rises.
- ❑ Turn on within 1s after PD is plugged in (single port only)
- ❑ Support ≤400mA loads for at least 50ms without current limiting—
  Disconnect on overcurrent (>350mA) between 50ms and 75ms
  Disconnect on undercurrent (<5mA) between 300ms and 400ms

PSE Operation

A PSE is required to probe the cable for the characteristic PD signature before applying voltage to the wire. A valid PD signature consists of a 25k resistor with up to three diodes in series with it, and no more than 0.11µF in parallel. The cable must be probed with voltages of less than 10V to minimize the chance of damaging a legacy data-only Ethernet device that may not be prepared to see 48V between its terminals. Only after a valid signature is detected may the PSE apply power to the wire.

After detecting a valid signature, a PSE may optionally check for a second PD classification signature that indicates the maximum power the PD will ever draw. This classification signature appears as one of several specific currents drawn by the PD when probed with a voltage between 15V and 20V. If the PSE opts to classify the PD, it can use the information to allocate power from a common power supply, or even deny power if it finds that the PD is requesting more than the PSE has available. The entire detection/classification/power up sequence must be complete within one second from the time the PD is first connected to the port.

Once the PSE has detected and optionally classified the PD and has decided to turn on the power, it must provide between 44V and 57V (nominally 48V) to the appropriate pairs on the cable. The port must be able to supply at least 400mA for 50ms without current limiting, and must be able to supply 15.4W (44V • 350mA). As the port voltage rises, the PSE may reduce the current limit it allows, as long as the 15.4W power level is maintained. The 15.4W requirement allows for a PSE operating at the minimum voltage (44V) to supply the full 12.95W a PD is allowed to draw, plus the drop through a worst-case 20Ω round-trip cable at the 350mA maximum continuous current. The port must limit output current to below 450mA at all times to protect against short circuits on the cable. If the PSE senses an overcurrent condition for more than 75ms, it must turn the power off.

Once the power is on, the PSE must keep it on as long as the PD presents a valid *power maintenance signature*. This power maintenance signature consists of two components, both of which the PD must exhibit: a minimum DC current draw of at least 10mA, and an AC impedance lower than 33kΩ at all frequencies from DC to 500Hz. The PSE can opt to monitor either or both components of this signature to determine if the PD is still present. If the PSE senses that the signature is invalid, it must wait between 300ms and 400ms before removing power from the line. The 300ms minimum prevents false disconnects caused by glitches on the line or sudden drops in the line voltage, and the 400ms maximum prevents a fleet-fingered technician

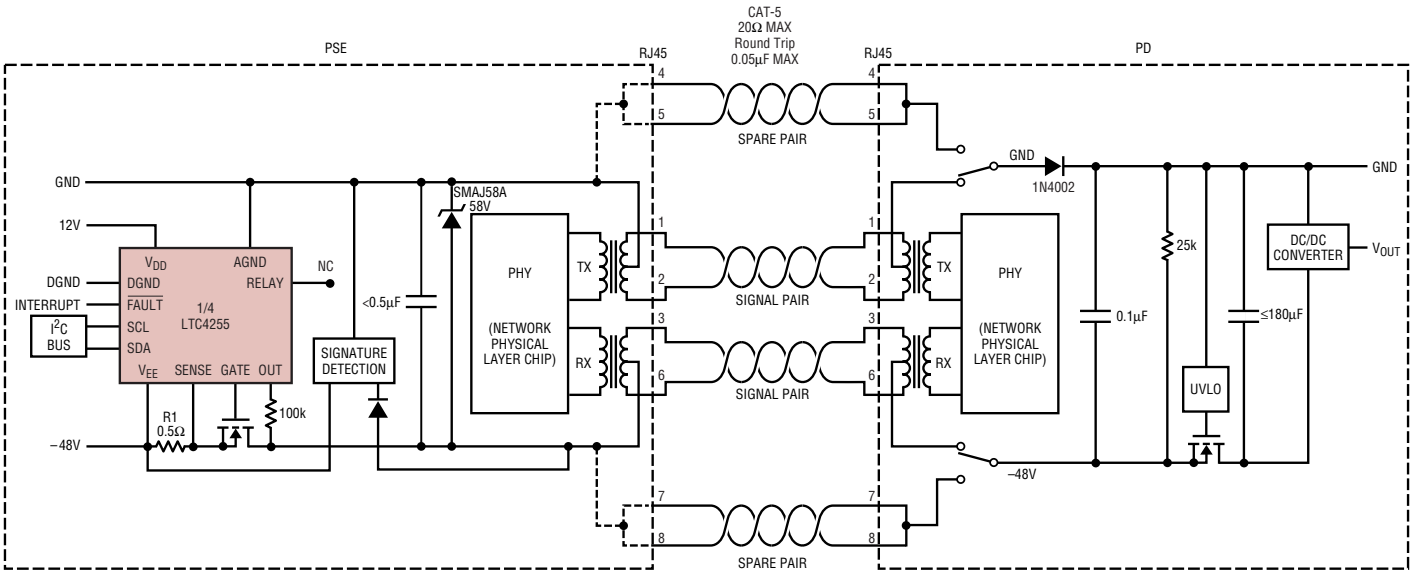


Figure 2. Power control circuitry using LTC4255 quad network power controller

from unplugging a valid PD and connecting a legacy device before the PSE has a chance to turn the power off.

LTC4255 Quad Network Power Controller

The LTC4255 is a quad –48V power controller, designed to implement the power path portion of a PSE device. It contains complete power management and switching circuitry for four channels, including –48V Hot Swap™ switching, current inrush control, current limit, and DC disconnect sensing for four ports. Internal status and control registers allow the LTC4255 to accept commands and report back status to the host system via the industry-standard two-wire I²C™ serial bus protocol. One LTC4255 channel, together with a standard differential data transceiver (commonly known as a "PHY"), a detection/classification circuit, and a couple of external components make a complete powered Ethernet port. The quad configuration of the LTC4255 makes it useful in multiport PSEs, such as powered Ethernet switches or hubs.

The primary function of the LTC4255 is to control the delivery of power to the PSE port. It does this by controlling the gate drive voltage to an external MOSFET (Figure 2) while monitoring the output current via sense resistor R1 and the voltage at the OUT pin. This circuitry serves to couple the raw –48V supply to the port in a manner than meets the PD's requirements while minimizing disturbances on the backplane.

When it receives an I²C bus command to turn on a port, the LTC4255 enters a timed startup mode where it powers up the PD in a mode that limits inrush current. The internal power control circuitry servos the gate drive to the external MOSFET to limit the port current, allowing the voltage at the port to rise in a controlled manner as the PD input capacitance charges. An internal timer controls the inrush duration, and foldback current limiting reduces the maximum current limit when the output voltage is below 30V, minimizing power dissipation in the external MOSFET. If the port reaches full voltage and the current draw drops below the current limit before the timer expires, the LTC4255 assumes the port turned on normally. It sets the Power OK bit in the status register and keeps the MOSFET gate turned fully ON until a disconnect or fault event occurs. If the port is still in current limit when the timer expires, the LTC4255 assumes there is something wrong with the PD, turns off the power and sets the corresponding fault bit in the status register.

Current Limit Protection

Once power has ramped up to its final value and the start-up timer has expired, the LTC4255 shifts to normal operation. In normal operation, the port current should never exceed the current limit level, I_{MAX}. The current limit circuit monitors the port current by watching the voltage across R1 and reduces the MOSFET gate voltage as needed to keep the current below I_{MAX}. When the current drops below I_{MAX}, the gate voltage is restored to the full value to keep the MOSFET resistance to a minimum.

If the port reenters current limit at any time after startup, a current limit timer starts. If this timer expires, the port is turned off and the fault bit is set in the corresponding power status register. The current limit timer is an integrating counter that decrements at a slower rate than it increments, preventing intermittent current limits from overheating the external power MOSFET.

DC Disconnect Detection

An additional current monitoring circuit trips when the port current drops below the minimum allowed level, signifying that the PD has been unplugged or has removed its power maintenance signature. If the current is still below the minimum when

continued on page 15

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High Speed Low Noise Op Amp Family Challenges Power and Distortion Assumptions with Rail-to-Rail Inputs and Output

by John Wright and Glen Brisbois

Introduction

The tradeoff is all too familiar; low noise op amps dissipate high power. The 1.9nV/√Hz LT6202, however, doesn't follow this rule. It provides rail-to-rail input and output operation (meaning that maximum dynamic range can now be extracted on low supply voltages) with a supply current of only 2.5mA. The LT6200 offers even lower noise (0.95nV/√Hz) and distortion, and it includes a shutdown feature for standby conditions. These unity gain stable amplifiers are well suited to fast low noise applications because of their respective 100MHz and 165MHz gain bandwidth, low distortion, guaranteed noise specifications, and low offset voltage. The amplifiers operate on a total supply voltage of 2.5V to 12.6V, and are fabricated on Linear Technology's high speed complimentary bipolar process. All are specified with 3V, 5V, and ±5V supplies. The single LT6202, dual LT6203 and quad LT6204 are identical except in the number of op amps; likewise for the single LT6200 and dual LT6201.

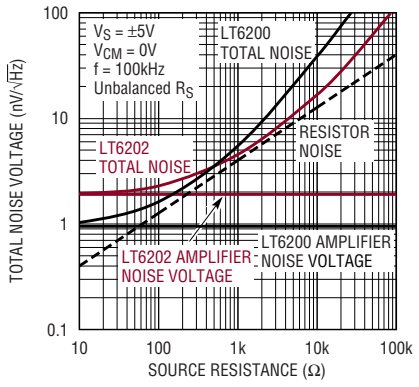


Figure 1. LT6200 and LT6202 total noise vs source resistance

Do the Math

The product of noise voltage and square root of supply current, $e_n \bullet \sqrt{I_{supply}}$, is a useful way to gauge the performance of fast low noise amplifiers. Amplifiers with low e_n have high $\sqrt{I_{SUPPLY}}$, and in applications that require low noise with the lowest possible supply current, this calculation proves to be enlightening. For example, the LT6202 has an $e_n \bullet \sqrt{I_{SUPPLY}}$ product of 3nV√mA/Hz, while the LT6200 $e_n \bullet \sqrt{I_{SUPPLY}}$ product is only 3.9nV√mA/Hz. It is common to see similar amplifiers with much worse $e_n \bullet \sqrt{I_{SUPPLY}}$ products of 4.1 to 13.2nV√mA/Hz.

An important consideration in applying the LT6200 is that noise of 0.95nV/√Hz is equivalent to the thermal noise of a 56Ω resistor. If the total source resistance exceeds this value, the source resistance dominates the noise of the circuit; not the noise of the LT6200. Figure 1 illustrates this effect by showing the total amplifier noise vs unbalanced source resistance. At low source resistance the total noise is dominated by the amplifier's noise voltage. When source resistance is between 56Ω and approximately 1.5kΩ, the noise is dominated by the resistor thermal noise. At high source resistance the total noise is set by the product of the amplifier noise current and the source resistance.

In the case of the LT6202, also shown in Figure 1, the source resistance conditions are less severe. The noise of 1.9nV/√Hz corresponds to the thermal noise of a 230Ω resistor. In the region between 230Ω and approximately 20kΩ the noise is dominated by the resistor thermal noise. Beyond this resistance the noise is set by the amplifier noise current. Below 500Ω of unbalanced source resistance, the LT6200 has lower total noise; above 500Ω, the LT6202 has lower total noise.

Low Noise and Low Distortion Design

An important rule of low noise bipolar amplifier design is that transistor noise voltage is proportional to the square root of the intrinsic base resistance r_b, and inversely proportional to the square root of the transistor operating current. This means that for low noise voltage the input transistors need to be physically large to reduce the r_b, and need to operate at high collector currents. In other words, halving the noise of the LT6202 requires input transistors four times larger operating at a minimum of four times the quiescent current, and this is exactly how the ultra low noise LT6200 was created. Additional current in the output stage is required to reduce the LT6200 distortion, shown in Figure 2, to an impressive –85dBc

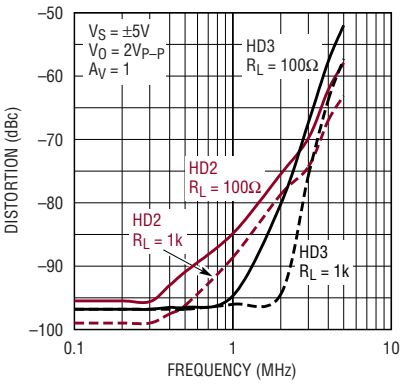


Figure 2. LT6200 distortion vs frequency

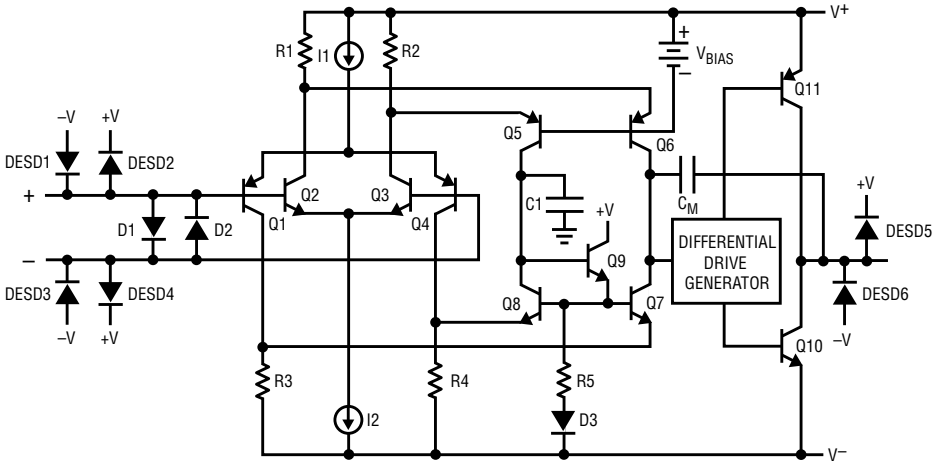


Figure 3. LT6200-4 simplified schematic

HD_2, and –95dBc HD_3 at 1MHz with R_L = 100Ω.

To see how these principles are applied, Figure 3 shows two parallel input stages of the op amps. This topology accomplishes several difficult tasks. First, PNP and NPN transistors in parallel reduce the effective r_b by a factor of 2 and the noise voltage by the $\sqrt{2}$. Second, the input stage can common mode from the positive supply to the negative supply. The trade off between low noise design and rail-to-rail input operation is evident in that higher collector current in Q1, Q2, Q3 and Q4 means lower noise voltage, but it also means a larger voltage drop across the collector loads R1, R2, R3 and R4, and less common mode range due to saturation of the input transistors. The input referred noise benefits further from high current in the second stage Q5, Q6, Q7 and Q8, but unfortunately this current further reduces the common mode range of the input stage. The saturation of the input transistors places an upper limit on operating currents and therefore amplifier noise.

When the common mode voltage is in the middle of its range, the input stage transconductance is set by both input pairs. As the common mode voltage approaches either supply, the positive rail for instance, I1 saturates and Q1 and Q4 cutoff. At this point the input g_m is reduced by half and is now set by Q2 and Q3 operating currents. With half the input stage g_m, the LT6202 offset voltage shifts by about 500µV, the gain bandwidth drops to 50MHz, and the noise voltage has the spectrum shown in Figure 4. The inputs can common mode to either rail, but as a practical matter for measuring noise the inputs must be taken a few hundred millivolts from the rails. The PNP stage alone has lower noise than the NPN stage alone, and this is attributed to lower r_b of the PNP transistors.

What about the ACs?

Capacitor C1 is used to reduce the input g_m versus frequency to avoid excess phase shift through the current mirror Q7 and Q8. This capacitor provides a single high frequency path to the collectors of Q6 and Q7. The compensation capacitor C_M produces a single pole open loop response, and lowers the AC output impedance.

There is a tradeoff between noise and slew rate in high speed amplifiers. The commonly used technique to obtain high slew rates is to reduce the input stage g_m by using input degeneration resistors, allowing for a proportional reduction in the compensation capacitor. Although this technique maintains the same gain bandwidth and yields a direct improvement in slew rate, it also causes a large degradation in the noise performance. For this reason, this family uses no input g_m reduction, favoring low noise over high slew rate. The slew rate and gain bandwidth could

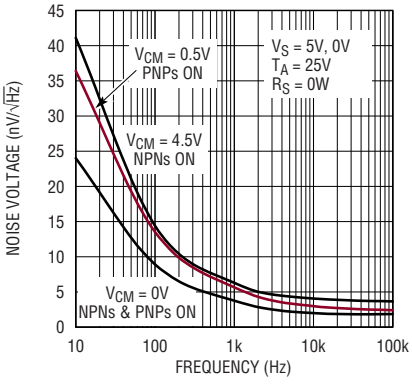


Figure 4. LT6202 noise voltage vs frequency

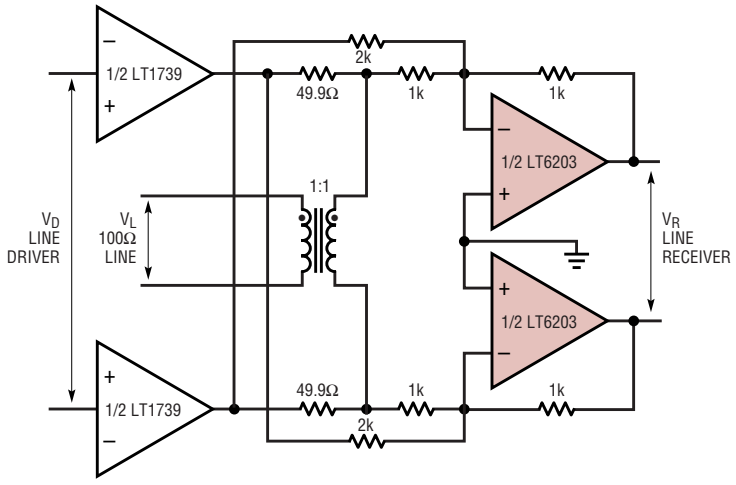


Figure 5. Low noise 4- to 2-wire local echo cancellation differential recieiver

also have been increased by reducing the compensation capacitor, resulting in the amplifier being stable only at closed loop gains >1. One reason, however, for making the amplifiers unity gain stable is to allow the closed loop gain to be rolled off with a feedback capacitor to further reduce the noise by limiting the bandwidth.

The LT6202 can drive capacitive loads as high as 100pF, while the faster LT6200 can drive 30pF. Table 1 shows a performance summary for both families.

Applications

Low Noise 4-Wire to 2-Wire Local Echo Cancellation Differential Receiver

Figure 5 shows a low noise 4-wire to 2-wire local echo cancellation differential receiver. With the LT1739 drivers in shutdown, the resulting noise is that of the LT6203 alone. The total integrated noise of the differential receiver is shown in Figure 6 from 25kHz to 150kHz.

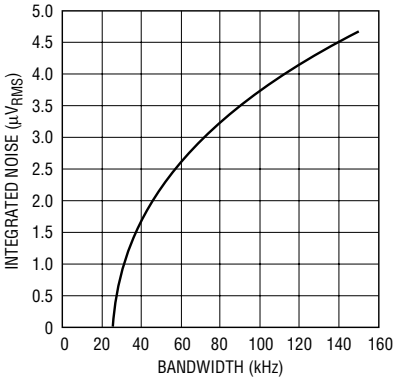


Figure 6. Line receiver integrated noise 25kHz to 150kHz

Table 1. LT6203/LT6204 Performance: T_A = 25°C, V_S = 5V, 0V unless otherwise specified.

			LT6200/LT6201			LT6202/LT6203/LT6204			
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Offset Voltage	$V_{CM} = V_S/2$			100	1000		100	500	μV
	$V_{CM} = V^+$ to V^-			0.6	2.0		0.8	2.0	mV
Input Bias Current				10	40		1.3	7.0	μA
Noise Voltage	f = 10kHz, V_S = ±5V			1.4	2.3		2.8	4.5	nV/√Hz
	f = 100kHz, V_S = ±5V			0.95			1.9		nV/√Hz
Noise Current	f = 10kHz	Balanced R_S		2.2			0.75		pA/√Hz
		Unbalanced R_S		3.5			1.1		pA/√Hz
Large Signal Gain	V_O = 0.5V to 4.5V, R_L=1k to $V_S/2$		40	70		70	120		V/mV
	V_O = 1V to 4V, R_L=100Ω to $V_S/2$		11	18		8	14		V/mV
Common Mode Rejection Ratio	$V_{CM} = V^+$ to V^-		65	90		60	83		dB
V_{OUT} Low	I_{SINK} = 20mA			150	290		240	460	mV
V_{OUT} High	I_{SOURCE} = 20mA			220	400		325	600	mV
Supply Current	Per amplifier			16.5	19		2.5	3	mA
Disabled Supply Current	V_{SHDN} = 0.3V			1.3	1.8		NA		mA
Gain Bandwidth Product	V_S = –5V, f = 1MHz			165			100		MHz
Slew Rate	A_V = –1, R_L=1kΩ, V_O = 4V		35	50		17	35		V/μs
Distortion	A_V = 1, 1MHz, $V_O = 2V_{P-P}$	HD2, R_L= 100Ω		–85					dBc
		HD3, R_L= 100Ω		–95					dBc
		HD2, R_L= 1k					–81		dBc
		HD3, R_L= 1k					–81		dBc

Single Supply, 1.5nV/√Hz, Photodiode Amplifier

Figure 7 shows a simple, fast, low noise photodiode amplifier. Feedback forces the BF862 JFET source to 2.5V, which causes the drain current to be 2.5mA. At this current, the V_{GS} of the JFET is about –0.5V, so the gate and output voltage both sit at about 2V DC and the photodiode sees 2V of reverse bias. Under illumination, the gate stays at constant DC voltage while the op amp output rises by $I_{PD} \bullet R_F$, giving the transfer function $V_{OUT} = 2V + I_{PD} \bullet R_F$.

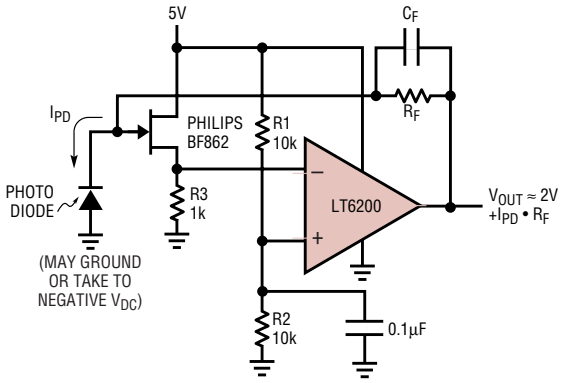


Figure 7. Single supply, 1.5nV/√Hz, photodiode amplifier

Amplifier input noise density and gain-bandwidth product were measured to be 1.5nV/√Hz and 157MHz, respectively, while consuming only 100mW. The reason the 165MHz gain bandwidth product of the LT6200 is not severely compromised by this composite circuit is that the JFET has a high g_m, approximately 1/50Ω, and looks into 1kΩ so loop attenuation is only 5%. Total circuit input capacitance including board parasitics was measured to be 3.2pF. This is less than the specified C_{GS} of the JFET, because the JFET source is not grounded but rather looks into R3 and the high impedance op amp input. This fact combined with the low input voltage noise makes the circuit well suited to both large and small photodetectors. The unity-gain stability and ultralow bias current of the circuit means that the transimpedance gain, set by R_F, can be any value from 10Ω to 10GΩ.

The circuit was tested using a small 2.5pF Advanced Photonix avalanche photodiode #012-70-62-541 reverse biased to –180V, and a 210kΩ feedback resistor R_F. This photodiode was selected for its speed, so that its inherent response would not impact the circuit bandwidth measurement. With feedback capacitance adjusted for 4% overshoot, closed loop bandwidth was measured to be 4.5MHz. This is in good agreement with theory given the ~5.7pF total input C and the 210kΩ transimpedance gain: 5.7pF is 6.2kΩ at 4.5MHz, for a noise gain of 210k/6.2k = 35, and a GBW product of 35 • 4.5MHz = 157MHz.

Available Packages

LT6200: SOT-23-6	SO-8
LT6201: SO-8	MSOP-8
LT6202: SOT-23-5	SO-8
LT6203: SO-8	MSOP-8
LT6204: SO-14	SSOP-16

Conclusion

Linear Technology's new family of low noise op amps operate rail-to-rail input and output while maintaining a light appetite for supply current. This combination is accomplished without sacrificing AC or DC performance. The family is available in singles, duals and quads and in a wide variety of packages.

LTC4255, continued from page 11

the disconnect timer runs out, the port power is turned off and the corresponding status bit is set. The LTC4255 monitors the DC component of the Power Maintenance Signature only; additional circuitry is needed to monitor the AC component of the signature if required by the application.

Conclusion

The LTC4255 provides complete power control circuitry to switch 48V onto Ethernet wires, greatly simplifying the design of the power path of PSE devices. An LTC4255, together with a standard quad PHY chip, a detection/classification circuit, and a handful of external components make four complete powered Ethernet ports. Fault protection, startup control, and disconnect sensing are all performed by the LTC4255, minimizing external circuitry. The I^2C interface simplifies monitoring and control of the LTC4255 by a host system.

Part 2 of this series will cover the details of PD design and show how to put together the power receiving end of the link.

Notes

[1] The 802.3af standard is still in draft form, and parts of the standard are still in flux. No product can yet claim full compliance, but compatible products are already available in advance of the final standard. For the latest information on the state of the 802.3af standard or on LTC products designed to meet the standard, contact the LTC Applications department.

Simplify Telecom Power Supply Monitoring with the LTC1921 Integrated Dual –48V Supply and Fuse Monitor

by Brendan Whelan

Introduction

The LTC1921 is the only fully integrated dual –48V supply and fuse monitor that meets common telecom specifications for supply range warning and that can withstand the high transient voltages required by telecom systems. This device improves system reliability by monitoring both supply inputs at the card edge and indicating the status of both supply fuses. The input pins are designed to withstand the large DC and transient voltages that may occur on the backplane supply. The outputs are designed to drive up to three LEDs or optoisolators, allowing warnings to be transmitted across an isolation barrier. The LTC1921 achieves high accuracy, high reliability and ease of use by combining an accurate internal reference, precision comparators and trimmed resistor networks in one package. Few external components are required, as shown in Figure 1, and none affect the threshold accuracy.

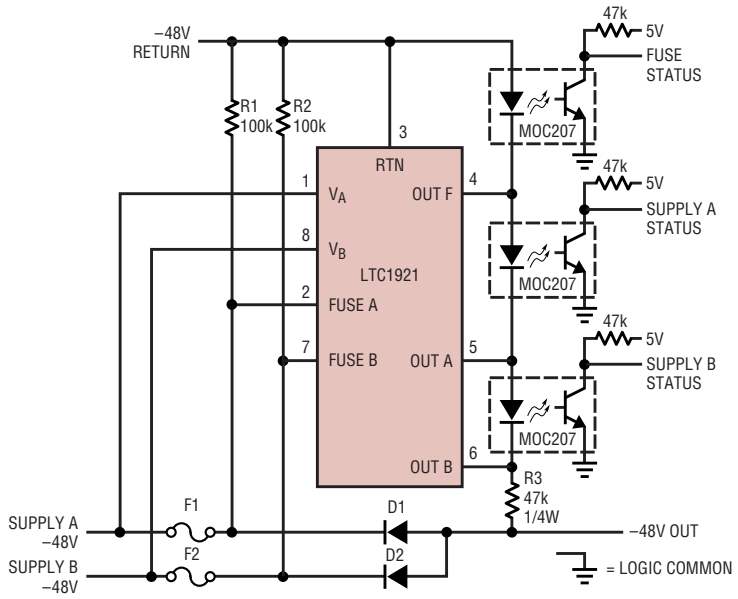
LTC1921 Features

- ❑ Independently monitors two –48V supplies for undervoltage (–38.5V ±1V_{MAX}) and overvoltage (–70V ±1.5V_{MAX}) faults
- ❑ Accurately detects undervoltage fault recovery: –43V±0.5V_{MAX}
- ❑ Monitors two external fuses
- ❑ Operates from –10V to –80V
- ❑ Tolerates DC faults to –100V
- ❑ Tolerates accidental supply reversal to 100V
- ❑ Withstands transient voltages up to 200V/–200V
- ❑ Small footprint: 8-lead MSOP and SO packages

How it Works

The LTC1921 monitors supply voltages by dividing the voltage internally and comparing the result to an internal precision reference. Since no precision external components are required, component cost, board space and engineering requirements are minimized, while accuracy is maximized. The LTC1921 comes with telecom industry accepted preset voltage thresholds, as illustrated by Figure 2, including undervoltage (–38.5V), undervoltage recovery (–43V) and overvoltage (–70V). The overvoltage threshold has a 1.3V hysteresis

...the LTC1921...can accurately provide warnings even if there is no power at all.



V_A	V_B	SUPPLY A STATUS	SUPPLY B STATUS
OK	OK	0	0
OK	UV OR OV	0	1
UV OR OV	OK	1	0
UV OR OV	UV OR OV	1	1

OK: WITHIN SPECIFICATION
OV: OVERVOLTAGE
UV: UNDERVOLTAGE

$V_{FUSE\ A}$	$V_{FUSE\ B}$	FUSE STATUS
$= V_A$	$= V_B$	0
$= V_A$	$\neq V_B$	1
$\neq V_A$	$= V_B$	1
$\neq V_A$	$\neq V_B$	1*

0: LED/PHOTODIODE ON
1: LED/PHOTODIODE OFF
*IF BOTH FUSES (F1 AND F2) ARE OPEN, ALL STATUS OUTPUTS WILL BE HIGH SINCE R3 WILL NOT BE POWERED

Figure 1: The LTC1921 requires few external components

that defines the overvoltage recovery threshold. These thresholds are trimmed to meet exacting requirements that are based on commonly used power supply specifications. This eliminates the need, as in the case of discretes, to calculate the aggregate error of a separate reference, multiple comparator offsets, and resistors. Internal resistors eliminate error due to board leakage, allowing the use of large internal resistor values that reduce power dissipation.

The LTC1921 is designed to indicate proper supply status over a wide range of conditions. In order to accomplish this, the internal architecture is symmetrical. The LTC1921 is powered via the supply monitor input pins, V_A and V_B, as shown in Figure 1. Supply current can be drawn from either or both pins, so the device can operate properly as long as at least one supply is within the operating range. Since power is not drawn from a combined supply (such as would be available with a diode OR), the LTC1921 will function properly even if the fuses or diodes are not functional.

A useful feature of the LTC1921 architecture is that it can accurately

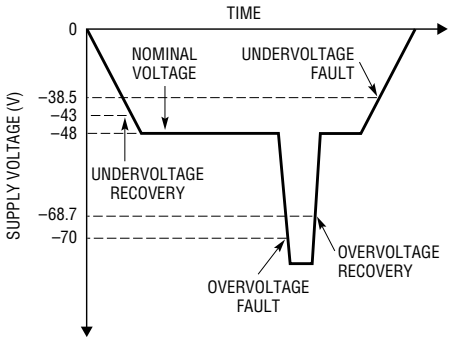
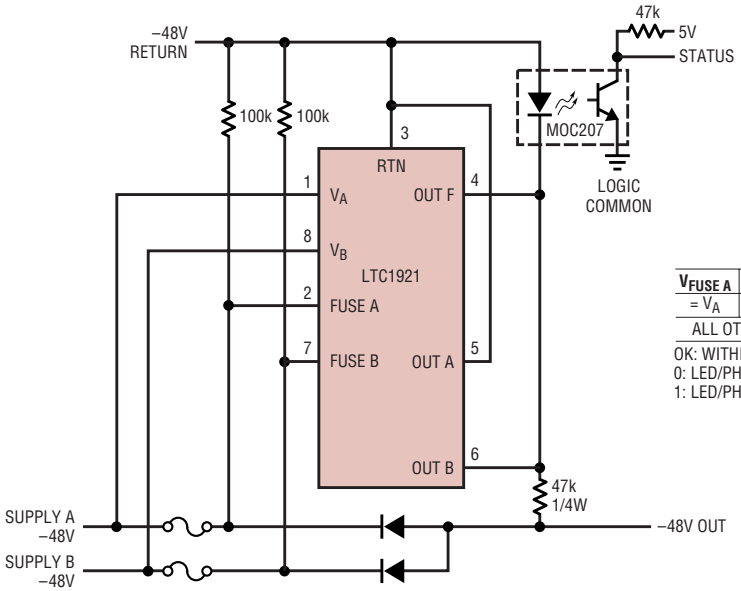
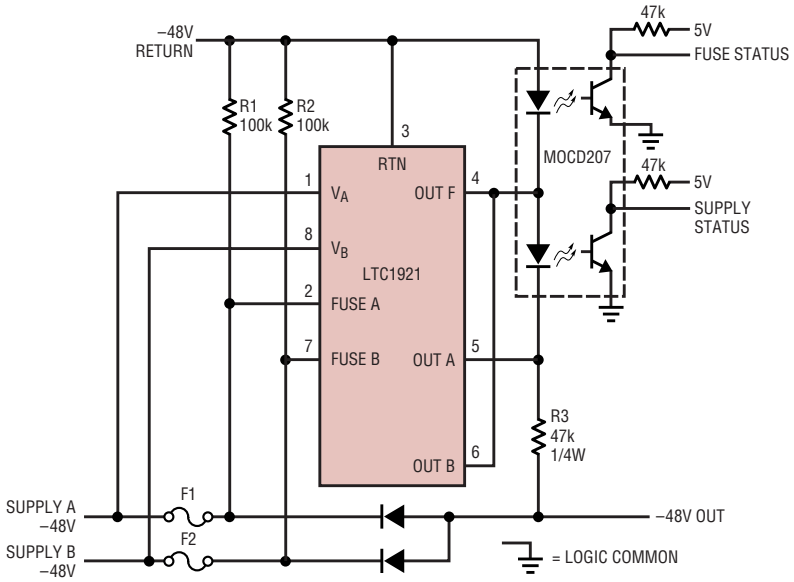


Figure 2: Voltage monitor thresholds



$V_{FUSE\ A}$ = V_A	$V_{FUSE\ B}$ = V_B	V_A	V_B	STATUS
		OK	OK	0
ALL OTHER CONDITIONS				1

OK: WITHIN SPECIFICATION
0: LED/PHOTODIODE ON
1: LED/PHOTODIODE OFF



V_A	V_B	SUPPLY STATUS
OK	OK	0
OK	UV OR OV	1
UV OR OV	OK	1
UV OR OV	UV OR OV	1

OK: WITHIN SPECIFICATION
OV: OVERVOLTAGE
UV: UNDERVOLTAGE

$V_{FUSE\ A}$	$V_{FUSE\ B}$	FUSE STATUS
= V_A	= V_B	0
= V_A	≠ V_B	1
≠ V_A	= V_B	1
≠ V_A	≠ V_B	1*

0: LED/PHOTODIODE ON
1: LED/PHOTODIODE OFF
*IF BOTH FUSES (F1 AND F2) ARE OPEN, ALL STATUS OUTPUTS WILL BE HIGH SINCE R3 WILL NOT BE POWERED

Figure 3: Output OR allows for fewer components

provide warnings even if there is no power at all. This is accomplished with a low voltage lockout circuit. If both supply voltages are very low, all three outputs of the LTC1921 lock into a fault indication state, thus communicating to supervisory systems that there is a power supply problem, even though the LTC1921 does not have enough power to maintain accuracy. As an example, if both supplies are active and fall below a magnitude of 13V, all outputs shunt until the supplies either recover or fall so low that the LTC1921 cannot keep its outputs shorted. At this point, the supply voltages are so low that the output diodes do not receive enough current through R3 (Figure 1) to turn on, so they continue to indicate a warning. The low supply lockout ensures that the LTC1921 provides proper warning if there is insufficient supply voltage to power its internal circuitry, and it occurs well below the undervoltage threshold of –38.5V, so supply warning accuracy is not compromised.

Finally, the LTC1921 is designed to monitor the supply voltages at the edge-connector, upstream of the series-connected supply diodes and fuses, which allows the LTC1921 to provide the most accurate assessment of supply condition possible.

LTC1921 monitors supply fuses F1 and F2, in Figure 1, by comparing the voltage potentials on each side of each fuse. This is accomplished by comparing the voltage at V_A (pin 1) to the voltage at Fuse A (pin 2) and the voltage at V_B (pin 8) to the voltage at Fuse B (pin 7). If a significant difference (about 2V) arises, the LTC1921 signals that a fuse has opened. The voltage difference across the damaged fuse may be reduced by diode reverse leakage, making it difficult to detect a damaged fuse. Weak pull-up resistors (R1 and R2, Figure 1) ensure that the voltage across a damaged fuse is sufficient for the LTC1921 to detect an open-circuit fuse. The size of these resistors is determined by the reverse leakage of the ORing diodes used in the application. The higher reverse leakage current exhibited by Schottky diodes may require lower-valued resistors to be used (as with R9 and R10, Figure 4).

The LTC1921 replaces complicated monitoring circuitry with a simple integrated precision monitoring system contained entirely in an MSOP-8 or SO-8 package.

The LTC1921 can communicate supply and fuse status by controlling external optoisolators or LEDs. This allows for intelligent system monitoring despite high isolation voltage requirements. Control of the LEDs or optoisolators is accomplished by connecting the LTC1921 outputs in parallel with the LEDs or photodiodes. During normal supply and fuse conditions, the LTC1921 outputs are high impedance: current flows through the external diodes continuously. If a fuse opens, or a supply voltage falls outside of the allowed window, then the proper LTC1921 output shunts the current around the diode, thus indicating a fault. The outputs have been designed to accommodate series connection of the output status diodes. This allows the use of one resistor (R3, Figure 1) instead of three, and cuts the total output current by the same factor. The outputs may be ORed to reduce the number of required optoisolators as shown in Figure 3. The supply outputs may be combined, or all outputs may be combined. The required warnings will be provided in all cases. The only difference in function is that the exact source of the warnings cannot be distinguished when the outputs are combined.

Application Example

Figure 4 shows an LTC1921 and an LT4250 Hot Swap controller comprising a complete telecommunications power system solution. The LTC1921 monitors both –48V supply inputs from the power bus, as well as the supply fuses. Because the LTC1921 measures both supplies at the card edge, it can provide warnings for conditions that other solutions cannot

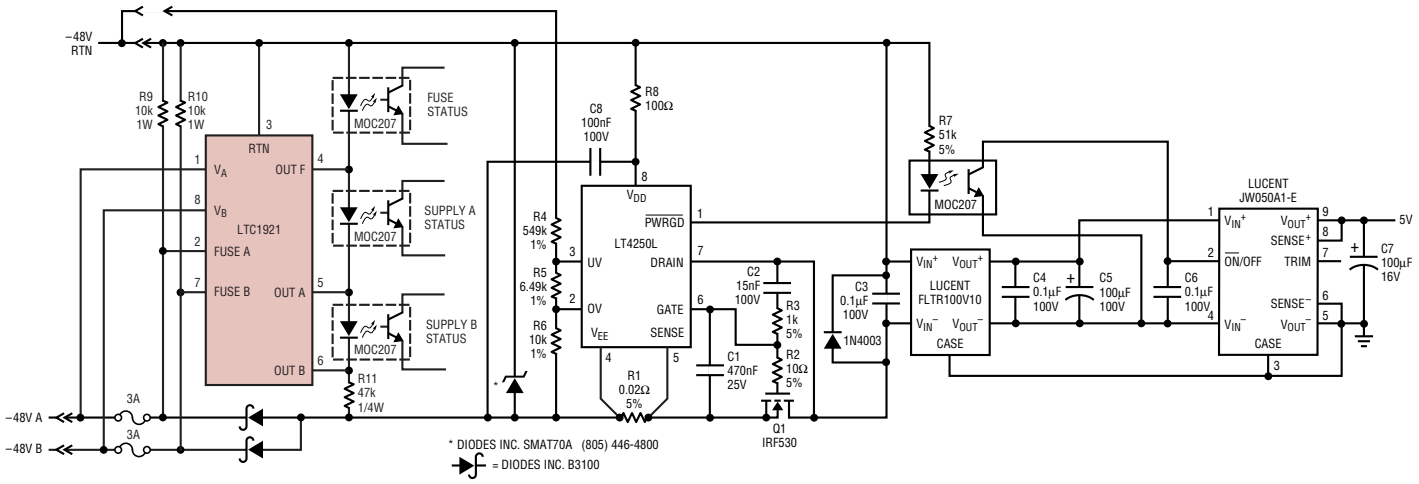


Figure 4: Network switch card application with Hot Swap control

measure, such as one supply failing or one fuse damaged. The supply measurement is also more accurate, since the voltage drop across the fuses or diodes does not affect it. Resistors R9 and R10 pull up the fuse pins so that damaged fuses can be detected. The status signals may be wired off the card, with optoisolators, to an isolated microprocessor or microcontroller that controls system performance and warning functions. This allows an automated system supervisor to issue a warning or record the event, despite operating from an isolated supply. The LT4250L switches the –48V supply via Q1 during hot swapping and low supply conditions, and monitors the supply voltage provided to the load. The PWRGD output of the LT4250 drives an optoisolator, providing a supply status signal to the DC/DC converter. This signal may also be used to monitor the condition of the ORing diodes by comparing it to the supply status signals from the LTC1921.

Conclusion

Reliability is top priority for the designers of modern telephone and communication equipment. Designers take extra care to protect circuitry from failure-causing temperature and voltage changes, employing redundancy whenever possible, especially for power supplies. They monitor supplies for early warnings of impending failure, often using complicated circuitry that can include a voltage reference, comparators, an LDO and several precision resistor dividers. Designers may also use discrete components to indicate the state of power supply fuses. The resulting circuits can be expensive in terms of component cost, board space and engineering time. The LTC1921 replaces this complicated monitoring circuitry with a simple integrated precision monitoring system contained entirely in an MSOP-8 or SO-8 package.

LT3430, continued from page 8

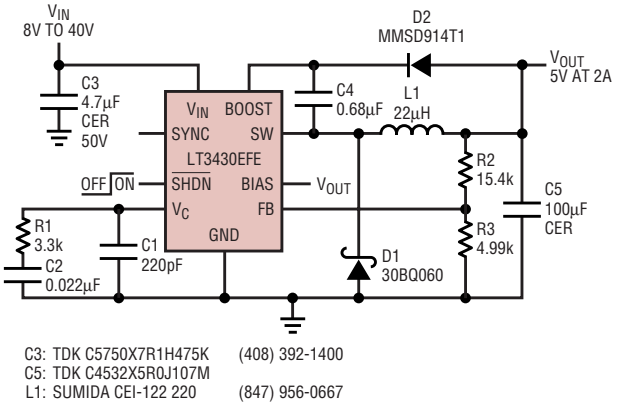


Figure 4. Low profile (max height of 3.0mm) FireWire peripheral supply with low output ripple voltage

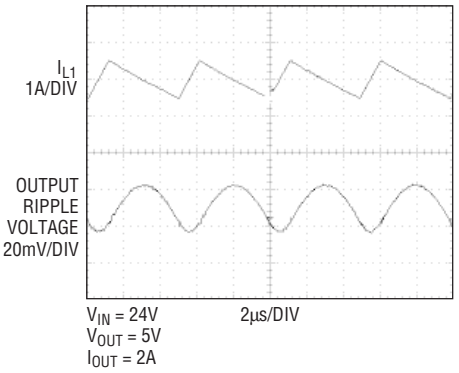


Figure 5. Output ripple voltage for the circuit shown in Figure 4

Figure 4 shows a 5V/2A solution for FireWire peripherals which takes advantage of the LT3430 current mode architecture by using a low ESR ceramic capacitor at the output. The circuit provides a low profile (all components less than 3.0mm height), low output ripple voltage solution. Output ripple voltage is only $26mV_{P-P}$, as shown in Figure 5, using a 22µH inductor, with V_{IN} = 24V and V_{OUT} = 5V at 2A.

Conclusion

The LT3430 features a 3A peak switch current limit, 100mΩ internal power switch and a 5.5V to 60V operating range, making it well suited to automotive, industrial and FireWire peripheral applications. It is highly efficient over the entire operating range, and it includes important features to save space and reduce output ripple—including a 200kHz fixed operating frequency, a current mode architecture and availability in a small thermally enhanced 16-pin TSSOP package.

Notes

[1] The 'no connect' pins 3 and 5 of the LT1766 and LT1956 must be connected for the LT3430 to handle the increased current in the SW output (pins 2 and 5) and the V_{IN} input (pins 3 and 4).

VRM8.5 Design with the LTC3720 Achieves Small Size and Fast Transient Response

by David Chen

Several different brands of CPUs fall into Intel® VRM8.5 category. Depending upon clock frequency and computation power, these CPUs consume different levels of supply current ranging from several amperes to 30A. The newly released LTC3720 single-phase PWM controller is designed for CPUs that consume up to 20A. It features a valley current control architecture that speeds up the VRM response to step load changes, two on-chip high current gate drivers for N-channel power MOSFETs, a current sensing mechanism that does not require an additional sense resistor and a 5-bit VID table that is compatible with Intel VRM 8.5. The resulting VRM 8.5 design has a small size and a fast transient response.

The LTC3720 also achieves a minimum on-time below 100ns and a wide input range from 4V to 36V. These are important characteristics for notebook CPU applications where the input-to-output ratio is usually high. Other LTC3720 features include a programmable current limit, an output overvoltage soft latch, a capacitor-programmable soft start, an

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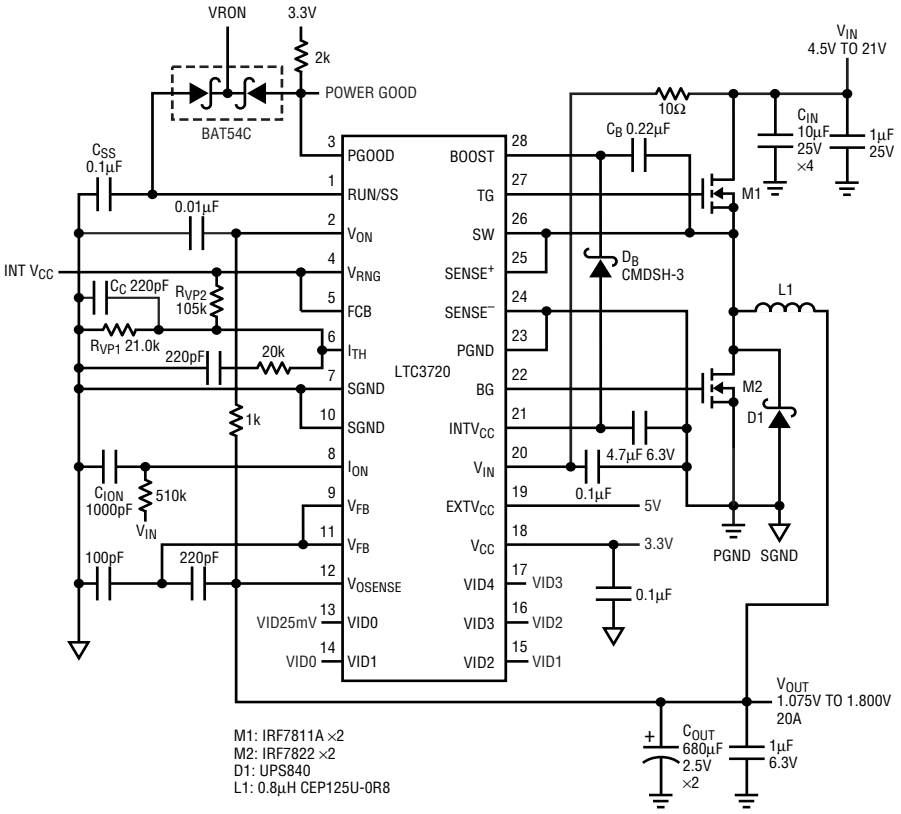

Figure 1. A 20A VRM8.5 design using the LTC3720

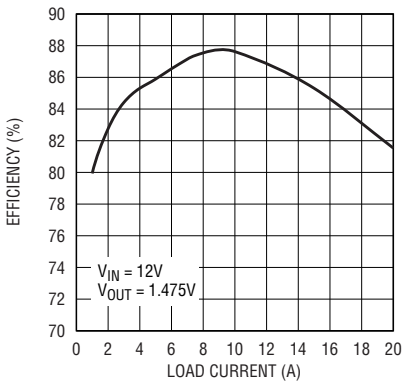

Figure 2. Better than 80% efficiency is achieved over a 1A–20A load range.

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High Performance Op Amps Deliver Precision Waveform Synthesis

by Jon Munson

Introduction

With the trend toward ever more precise waveform generation using DSP synthesis and digital-to-analog conversion, such as with the LTC1668 16-bit, 50Msps DAC, increasing demands are being placed on the output amplifier. In some applications, the DAC current-to-voltage function is simply resistive, though this is limited to small-signal situations. The more common solution is to use an amplification or a transimpedance stage to provide larger usable scale factors or level shifting. Figure 1 shows one such example, with an LT1722 performing a differential-current to single-ended-voltage amplification for an LTC1668.

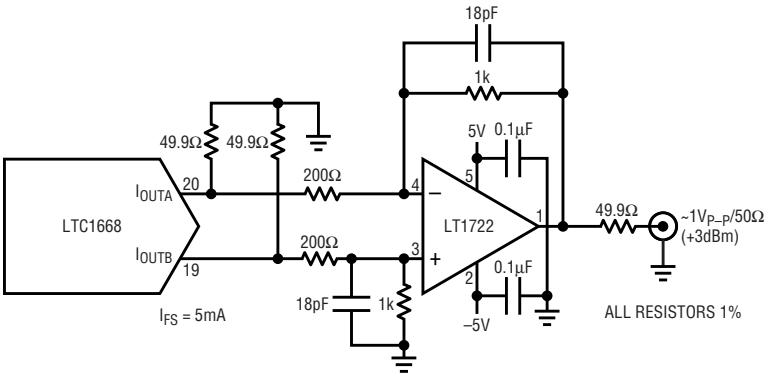

Figure 1. Differential-current to single-ended-voltage DAC amplifier

The LT1722, LT1723 and LT1724 Low Noise Amplifiers

The LT1722, LT1723 and LT1724 are single, dual and quad operational amplifiers that feature low noise and high speed along with miserly power consumption. The parts are optimized for low voltage operation and draw only 3.7mA (typical) per section from ±5V supplies, yet deliver up to 200MHz GBW and quiet 3.8nV/√Hz, 1.2pA/√Hz (typical) noise performance. DC characteristics include sub-millivolt input offset precision and output drive greater than 20mA, excellent for cable driving. The LT1722 single is also available in a SOT-23 5-lead package making it easy to fit into PCB layouts.

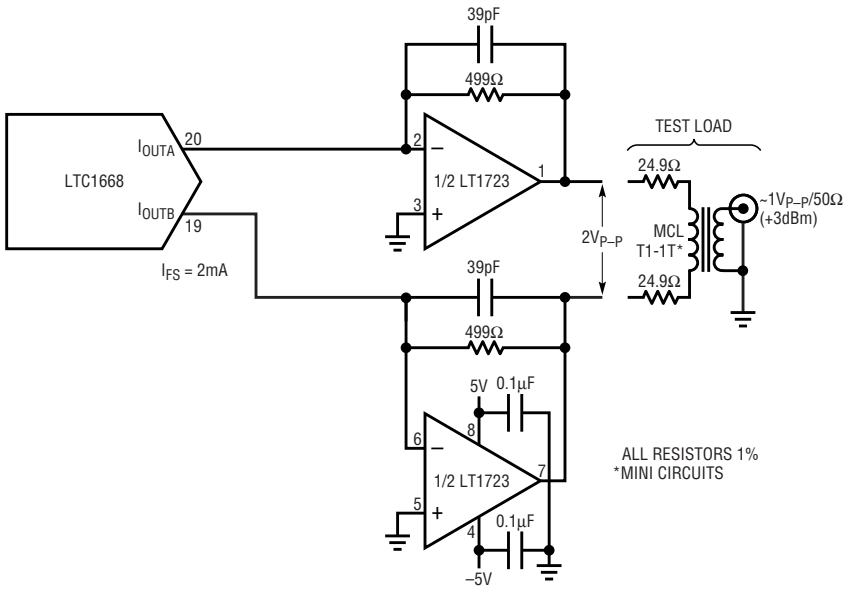

Figure 2. Twin transimpedance differential-output DAC amplifiers

DAC Output Amplifier

The circuit in Figure 1 provides ±1V at the amplifier output pin for full-scale DAC currents of 5mA, therefore offering, with the 50Ω series termination shown, a +3dBm sine-wave drive into a 50Ω load (~$1V_{P-P}$). In this particular configuration, the LT1722 is operating at a noise-gain of 5, and provides a small-signal bandwidth of about 8MHz (–3dB). The amplifier contribution to output noise is approximately given by

$$e_n G_n \sqrt{BW} = 3.8 \bullet 10^{-9} \bullet 5 \bullet \sqrt{8 \bullet 10^6} = 54\mu V$$

for the circuit as shown (resistor noise will increase this to about 75µV). With 16-bit resolution, a one LSB increment at the amplifier output is 31µV, so therefore the LT1722 amplifier noise will have only minimal impact on the available dynamic-range of the converter.

Some applications require amplified differential outputs, such as driving Gilbert-cell mixers (such as the LT5503 IQ modulator) or RF trans-

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Lower the Output Voltage Ripple of Positive-to-Negative DC/DC Converters with Optimum Capacitor Hook-Up

by Keith Szolusha

Low ripple voltage positive-to-negative DC/DC converters are used in many of today's high frequency and noise sensitive disc drives, battery powered devices, portable computers, and automotive applications. A positive-to-negative converter can have very low output ripple voltage (similar to a typical buck converter) as long as the bulk input capacitor is placed between V_{IN} and V_{OUT}, as opposed to placing it between V_{IN} and ground. There is a common misconception that positive-to-negative converters in the former configuration have noisy outputs, but this configuration actually solves noise problems rather than introducing them. In either configuration (as shown in Figures 1a and 1b) the V_{IN} and GND pins of an LT1765 are connected to V_{IN} and V_{OUT} respectively. Therefore, placing the input capacitor between V_{IN} and V_{OUT} is equivalent to placing it between the LT1765's V_{IN} and GND pins (as shown in Figure 1a). The other, commonly accepted method of placing the bulk input capacitor between V_{IN} and ground (as shown in Figure 1b) significantly increases the output voltage ripple (see Figures 2a and 2b). To make matters worse, this configuration requires an additional high-frequency bypass capacitor between the V_{IN} and GND pins of the IC.

In simple positive-to-negative converters, like those shown in Figures 1a and 1b, the output voltage ripple is:

$$\Delta V_{OUT(P-P)} = ESR_{COUT} \bullet \Delta IC_{OUT\ (P-P)}$$

Low ESR output capacitors, such as ceramics, help to minimize the output voltage ripple in DC/DC converters. For a given output capacitor ESR, output voltage ripple can be further reduced by minimizing the current ripple that the output capacitor is forced to absorb. In Figure 1b, the output capacitor is part of the high dI/dt switching current path, making the output voltage ripple proportionately larger.

With the bulk input capacitor placed as shown in Figure 1a, the peak-to-peak ripple current in the output capacitor is equal to the peak-to-peak ripple current in the inductor, which is designed to be relatively low for continuous-mode operation.

$$\Delta I_{COUT(P-P)} = \Delta I_{L(P-P)} = (V_{IN} \bullet \text{Duty Cycle})/(f_{SW} \bullet L)$$

where:

$\Delta I_{COUT(P-P)}$ = output cap ripple current
$\Delta I_{L(P-P)}$ = inductor ripple current
f_{SW} = switching frequency

When the bulk input capacitor is placed as shown in Figure 1b, the peak-to-peak ripple current in the

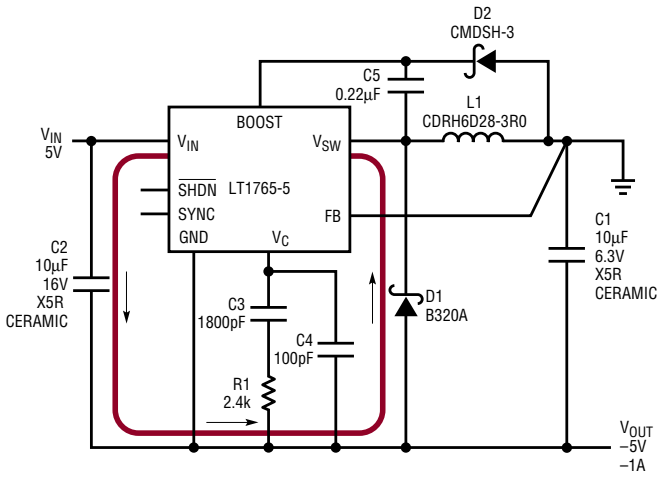

Figure 1a. LT1765 5V to –5V converter with bulk input cap between V_{IN} and V_{OUT} (IC GND pin) has low output ripple. The high dI/dt path, indicated here with bold red lines, does not include the output capacitor.

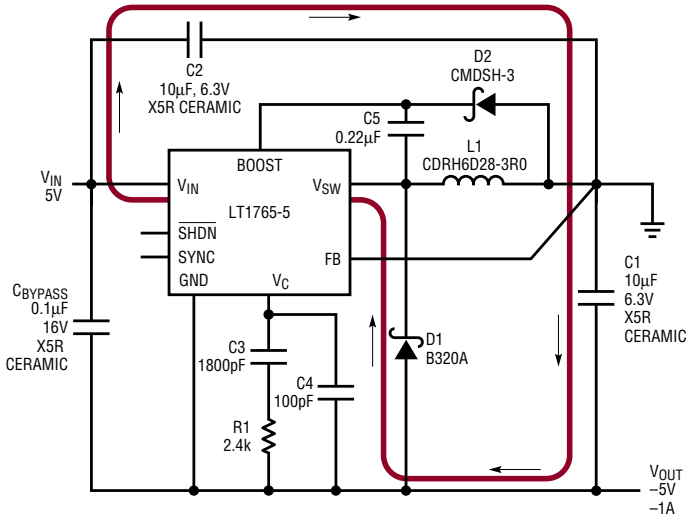

Figure 1b. LT1765 5V to –5V converter with the bulk cap between V_{IN} and ground has much higher output ripple than the circuit in Figure 1a. The high dI/dt path, indicated here with bold red lines, includes the output capacitor, thus increasing output ripple.

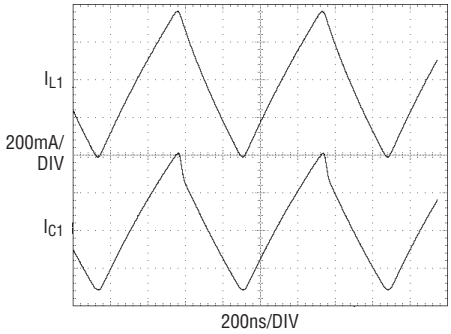

Figure 2a. In the circuit shown in Figure 1a, the output capacitor (C1) peak-to-peak current ripple is equal to inductor peak-to-peak ripple with 1A output.

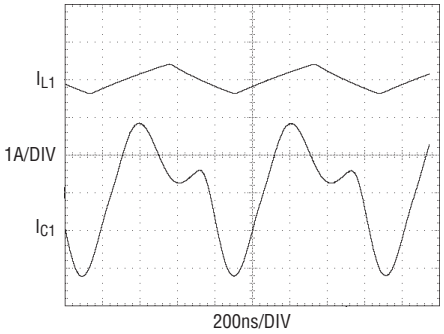

Figure 2b. In the circuit shown in Figure 1b, the output capacitor (C1) peak-to-peak current ripple is five times as high as inductor peak-to-peak ripple (and therefore five times as high as the current ripple shown in Figure 2a) with 1A output.

output capacitor is much higher than the inductor's ripple current alone; it is almost equal to the inductor's ripple current plus the input capacitor's ripple current.

$$\Delta I_{CIN(P-P)} = I_{L(P)} = I_{OUT} + I_{IN} + \Delta I_{L(P-P)}/2$$
$$\Delta I_{COUT\ (P-P)} \sim \Delta IL_{(P-P)} + \Delta I_{CIN(P-P)}$$

With much lower output capacitor ripple current, the size of the output capacitor in the circuit shown in Figure 1a can be much smaller than that of the circuit shown in 1b. Also, it does not need to handle nearly as much RMS ripple current (approximately equal to peak-to-peak ripple current divided by the square root of twelve).

Another advantage of removing the output capacitor from the high dI/dt switching loop (by judicious placement of the input capacitor) is that the layout is greatly simplified. The high dI/dt components shown in Figure 1 must be placed in the smallest loop possible to minimize trace inductance and the resulting voltage (noise) spikes. With one less component to worry about in the layout, it is easier to create a noise-free circuit using the layout shown in Figure 1a than it is using the one shown in Figure 1b.

Conclusion

Instead of placing the bulk input capacitor between the input supply and ground, place it across the input and ground pins of the step-down converter IC such as the LT1765. The result is significantly lower voltage ripple at the output and a simpler circuit design.

LT1722, continued from page 21

formers. For such applications the LTC1668 differential current outputs can be amplified with twin transimpedance stages as shown in Figure 2, which offers the opportunity to reduce the DAC current without loss of signal swing.

The circuit shown has the DAC full-scale currents reduced to 2mA to achieve a substantial power savings over the standard 10mA operation. The scale factor of the transimpedance amplifiers is set to provide $2V_{P-P}$ differentially. Operating at a noise-gain of unity, this circuit provides a small-signal bandwidth of about 12MHz (–3dB). The noise contributed by the LT1723 amplifiers to the differential load is approximately

$$\sqrt{2}e_nG_n\sqrt{BW} =$$
$$\sqrt{2} \bullet 3.8 \bullet 10^{-9} \bullet 1 \bullet \sqrt{12 \bullet 10^6} = 19\mu V$$

for the circuit as shown (the resistors in the circuit will add some additional noise bringing the total to about 24µV). This compares favorably with the nominal 16-bit LSB increment of 31µV, thus barely impacting the converter dynamic range.

The common mode output voltage of the circuit in Figure 2 is fixed at 0.5V DC, though some loads may require a different level if DC-coupling is to be supported, such as when soft-controlled offset nulling is required. Though not shown here, specific matched currents can easily be introduced to the inverting-input nodes of the two amplifiers to provide common-mode output control.

Each of the amplifier circuits presented will deliver +3dBm into 50Ω with harmonic distortion products below –60dBc for a synthesized full-scale fundamental of 1MHz. The nominal feedback capacitances shown provided ~1% step-response overshoot in the author's prototype configuration, but as with all amplifier circuits, some tailoring may be required to achieve a desired rolloff characteristic in the final printed-circuit layout.

Conclusion

When considering candidate devices for DAC post-amplification, it is important to consider the noise contribution. The LT1722 family of devices offers the low noise and wide bandwidths demanded by modern 16-bit waveform synthesizers, particularly those used for vector modulation, where high-fidelity is paramount.

Additionally, the particularly low noise characteristics of the LT1722, LT1723 and LT1724 op amps provide optimal noise performance for external impedances ranging from several hundred ohms to about 12kΩ, making these parts ideal for a variety of precision amplification tasks.

Use a Single Input to Acquire Two Similar Signals Simultaneously and Other AC Techniques for the LTC1864

by Derek Redmayne and Mark Thoren

If you have the processing power of a digital signal processor available, the LTC1864 ADC has the AC performance necessary to simultaneously digitize two signals in the 60Hz to 50kHz range. This technique allows you to retain the 250kHz sample frequency whereas multiplexing two channels would cut the sampling frequency in two. The technique described here uses the region near Nyquist for a second measurement channel, assuming the use of an FIR filter will suppress this region in the case of the first channel.

In Figure 1 the second channel (f2) is modulated with Nyquist frequency ($1/2 \bullet f_S$) in order to make it appear at Nyquist – f2. The subsequent digital processing of this second channel involves inverting every other sample to invert the entire spectrum, restoring the original frequency of f2, and making f1 appear near Nyquist. The frequency range of the individual channels must roll-off significantly before Nyquist, either by use of a filter, or due to naturally occurring phenomena such as a vibration that tends to roll-off at between 12 and 18 dB per octave.

The frequencies of interest in the two data paths can be isolated by the use of either identical or specifically tailored FIR filters. The two frequencies in the example are at 5.065kHz, and 4.883kHz; 183Hz apart.

The 250ksps sampling rate allows the use of simple 1st or 2nd order antialiasing filtering to measure lower frequency physical phenomena such as vibration. This, in addition to being less costly than a higher order anti-aliasing filter, may make it possible to implement a more nearly ideal overall pass band characteristic using a digital FIR to define cut-off rather than a physical filter. A higher sample frequency relative to the band of interest will allow the use of an FIR filter having some combination of lower pass band ripple, sharper roll-off, better phase linearity, less delay or better stop-band rejection. A higher sample frequency allows a longer FIR filter for a given latency, and when the pass band is a small fraction of the Nyquist frequency, nonideal artifacts resulting from the use of an FIR filter with noncoherent frequencies are reduced.

By using a sample frequency significantly greater than the frequency range of interest, it is possible to extend resolution beyond the resolution of the converter. DNL can be reduced using dither, but INL is no better than that of the converter.

For example, an increase in sampling frequency from 44kHz to 220kHz, a factor of 5 increase, results in improvement in signal to noise

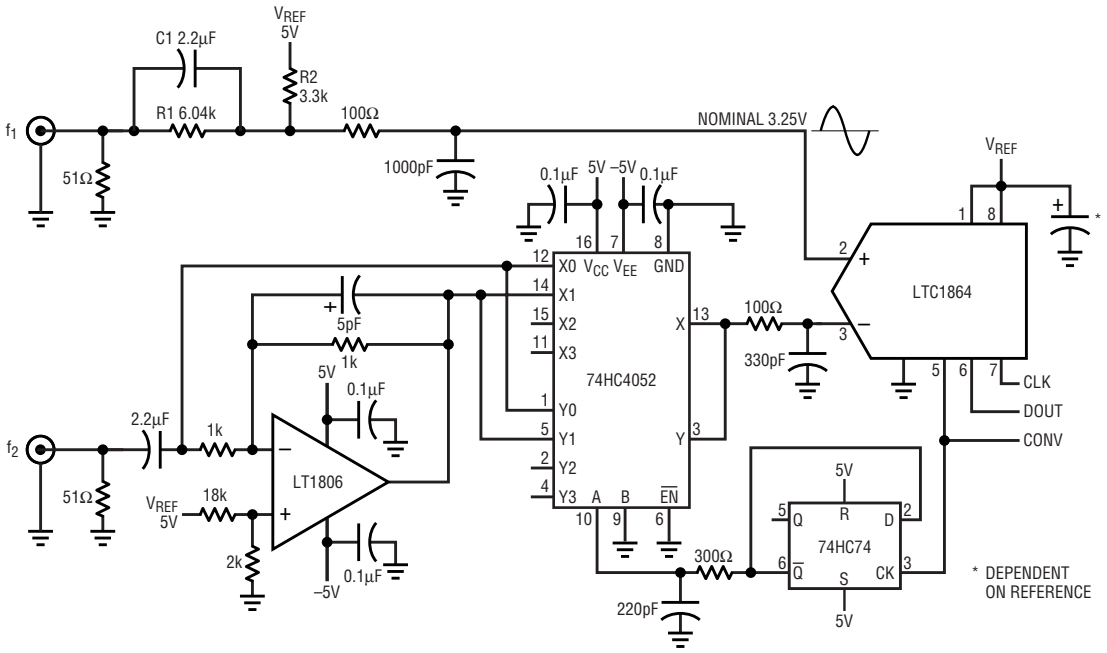

Figure 1. Second frequency modulated with Nyquist frequency

ratio is proportional to the square root of 5, or 7dB.

If the primary measurement function is related to the DC to 20kHz range, and if the intent is to implement an FIR filter in any case to produce a suppression of higher frequency components, decimation filtering or to provide programmable cut-off frequencies, you may want to consider using the region near Nyquist (fs/2) for a second signal. This second signal could be the result of excitation of a sensor at or near Nyquist, or this signal can fall into the same DC to 20kHz range and be modulated by a mixer at Nyquist.

In the case of the LTC1864, this second signal can be driven into the second (inverting input) as if it were simply a second input (see Figure 1). If a larger number of sensors were required, it may be better to sum as many as 20 or 30 inputs into a single high performance low noise amplifier such as the LTC1468 (see Figure 2)

In the first case, the second signal is modulated at Nyquist by using an analog multiplexer alternating between inverted and noninverted signal paths.

The subsequent sample processing involves inverting every other sample, and running this sample stream through possibly the same FIR filter algorithm as is used for the first channel. This action of inverting every other sample in the digital domain converts this signal back to its original frequency region. In this second representation of the input data, the lower frequency content associated with the first channel then appears near Nyquist. The FIR filter can be optimized to maximize suppression in the region approaching Nyquist.

As the samples defining these two signals are taken at exactly the same time, there is no differential delay between the two signals. The samples are effectively simultaneous.

Relative to a true simultaneous sampling converter this approach of using a single channel may save money on the converter and the cost of the serial interface.

An equivalent 2-channel scheme would require 500ksps or an average data transfer of somewhat higher than 8 Mbps.

Why is this better than multiplexing the two signals in a conventional manner? It is better primarily because it leaves Nyquist at 125kHz rather than halving it to 62.5kHz. If the second channel requires lower resolution, the loss of dynamic range on the first sample is minimal, and in fact, the second may act as dither for the first.

If the amplitude of the input signals falls off naturally with frequency, this approach could be used to acquire two signals with relatively flat response to 50kHz as the antialiasing filter then does not require a steep roll-off.

As the two signals will add, the maximum input signal for each is limited to –6dBfs unless they are unequally weighted, or unless the simultaneous occurrence of high-level signals is impossible.

Circuit Description

Figure 1 shows f1 passing through a level-shift bias circuit that raises the nominal input voltage at pin 2 to 3.25V to optimize the input range for AC, assuming that the inverting input (pin 3) is at a nominal bias voltage of 0.5V. R1 would be 6.04K, and R2 would be 3.32K for this example. If this input is to be used for DC in the 1V–5V range, these resistors are not necessary. The biasing of the LT1806 produces a nominal output voltage of 0.5V.

These values are assuming the maximum signal at f1 is –3dBfs, and f2 is –15dBfs. If –15dB seems low, narrow band filtering performed on f2 can produce good SNR.

In other examples of reuse of frequency spectrum, Nyquist frequency can be used to excite sensors from thermistors to capacitive proximity sensors, or inductive sensors. The use of AC can be used to sense across a large potential difference, for example, chopping a small current sense voltage sitting at 150V, and AC coupling the resulting signal using a capacitor rather than using an expensive isolated subsystem. Yet another example may involve optical excitation at Nyquist.

In another example (Figure 2), a large number of capacitive proximity sensors can be summed, but the total signal must not exceed full scale. In the case where 32 channels are summed, the maximum signal level on any channel must be –30dBfs unless the simultaneous occurrence of all signals is prevented.

This use of a large number of channels using AC frequency components can be isolated from each other using either an FFT, or a series of Discrete Fourier Transforms (DFT) tailored to each frequency. The advantage of the DFT is that less memory is required, and it can be done as the samples are acquired, as opposed to the very orthogonal FFT that requires that all

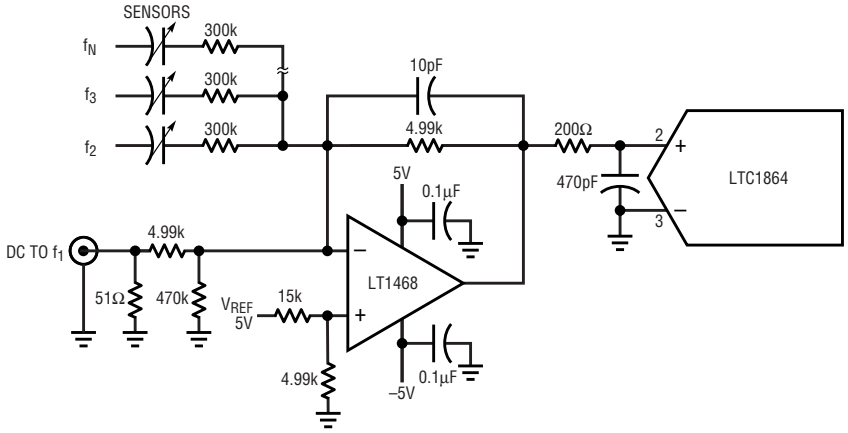

Figure 2. Using a large number of sensors

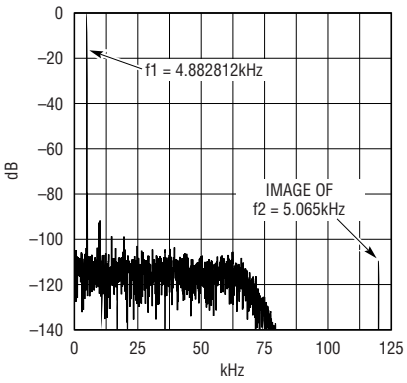

Figure 3. Primary measurement function, DC–50kHz

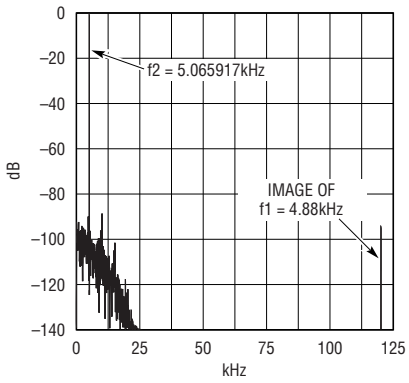

Figure 4. Secondary channel translated from 120kHz to 5kHz

samples be available before the algorithm is begun. The DFT however quickly becomes impractical beyond isolating a few frequencies.

In these cases where many excitation frequencies are used[1] and distinguished by transforming into the frequency domain, the frequencies should be "coherent" with the sample window. This means that there are an exact integral number of sinusoids of each frequency in the sample window. The Fourier transform performs a series of array multiplications that essentially down-convert (mix) each sine and cosine (real and imaginary) component to DC. The amplitude of each frequency component (bin) in the Fourier transform is then calculated by summing the power of the sine and cosine components. If these frequencies are coherent, this works very well. If there is not an exact match between input frequencies and those used in the algorithm, there are effects referred to as leakage. Leakage appears to raise the noise floor around a noncoherent frequency, and potentially masks details. With a large number of noncoherent frequencies, the transform becomes unusable.

If the frequencies used are not coherent, the use of windowing can reduce the leakage that results from an FFT performed on frequency components that are not an exact match for those frequencies that are used in the transform. Windowing involves first applying a symmetrical profile to the data set that tapers the weighting of the samples towards each end, reducing the error contribution of any discontinuity at either end of the sample set. The sample set can be viewed as a repeating waveform and a discontinuity would repeat at f_S/N_{FFT}. The windowing is akin to AM modulation, and hence has side lobes around each component.

A group of 32 capacitive sensors could be used for various tasks such sensing the position of some object routed through a series of sensors; measuring the flatness of a surface; or the dielectric constant of some material compared to reference material; or detecting the presence of objects in material handling devices.

Figure 3 and Figure 4 show the output of a 4096 point FFT performed on the output of two FIR filters processing the two data streams.

Figure 3 is the result of a 32 tap FIR low pass filter with –3dB at 50% Nyquist on the original sample set. Figure 4 is the result of inverting every other sample in another set, which is subsequently passed through an FIR filter with a corner frequency at 10% of Nyquist. In Figure 3 the first channel is at –4dBfs, and the secondary channel is at –15dBfs.

The signals that are processed in the secondary frequency range near Nyquist should be reduced in amplitude relative to the primary channel, in order to avoid reducing the dynamic range of the primary function.

This approach can be used for a large variety of secondary measurement tasks where the frequency range near Nyquist is suppressed by digital signal processing of the over-sampled signals.

Conclusion

The use of the LTC1864 for simultaneous acquisition of this type can provide a higher level of functionality without significant cost, or power implications. Portable or loop powered remote applications, constrained by a severely restricted power budget, can maintain the continuous sampling of the ADC while periodically using the secondary measurements at a low duty cycle or using a multiplexer to expand the number or measurements. The measurements in the secondary channels do not in this case disturb the deterministic operation of the primary channel.

NOTES

[1] An FPGA can be a compact and inexpensive way of building a large number of phase lock loops in order to produce a reasonable collection of excitation frequencies that are all coherent.

This can be done by dividing the sample clock by 2^N, where 2^N is less than the size of the FFT, to produce a reference frequency (f_{REF}) in a range that is noninterfering, and manageable in terms of VCO tuning range, and which also results in manageable loop filters. The VCO operates at an integer multiple of f_{REF}. Subsequently, the output of the VCO must be divided by (FFT Size)/2^N, where 2^N is the same as above.

For example, for a 1024-point FFT, a divide by 8 of the sample frequency will produce 31.250 kHz from the 250kHz sample clock. This can be the frequency at which all the phase comparators operate. The phase lock loops would each have a VCO divided by an integral number related to the bin number. The output of each VCO would also have a divider at (1024/8) = 128 to produce the coherent excitation frequency. For example, for an excitation frequency 1 bin before Nyquist, the VCO would operate at 31.96875MHz, and the excitation frequency would be at 249.7558kHz. This frequency is not necessarily the best choice of frequency, it is just an example.

If the frequency range of interest of the primary function is limited to a few kHz—as is often the case with pressure, load, temperature, etc.—a range of frequencies that may be better suited to capacitive sensors could be used, or for example, in the range of 50kHz. For example, a group of 32 coherent frequencies, preferably falling in odd bin numbers, could be produced in the range of 53kHz–73kHz. The 3rd harmonics of this group will fall unobtrusively in the range of 94kHz–123kHz.

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2.5A, 4MHz Monolithic Synchronous Regulator Offers a High Efficiency, Compact Solution by Reducing External Component Count and Size

by Joey M. Esteves

Introduction

The LTC3412 offers a compact and efficient voltage regulator solution for portable electronics that require low supply voltages (down to 0.8V) from a 3.3V to 5V power bus. Internal power MOSFET switches, with only 85mΩ on-resistance, allow the LTC3412 to deliver up to 2.5A of output current with efficiency as high as 95%. The LTC3412 saves space by operating with switching frequencies as high as 4MHz, permitting the use of small inductors and capacitors.

The LTC3412 employs a constant frequency, current mode architecture that operates from an input voltage range of 2.625V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 2.5A of output current. The switching frequency can be set between 300kHz and 4MHz by an external resistor. The LTC3412 can also be synchronized to an external clock, where each switching cycle begins at the falling edge of the external clock signal. Since output voltage ripple is inversely proportional to the switching frequency and the inductor value, a designer can take advantage of the LTC3412's high switching frequency to use smaller inductors without compromising output voltage ripple. Lower inductor values translate directly to smaller physical inductor case sizes, reducing the overall size of the system.

OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of loads and output capacitors, including ceramics. For increased thermal handling, the LTC3412 is offered in a 16-lead TSSOP package with an exposed pad to facilitate heat sinking.

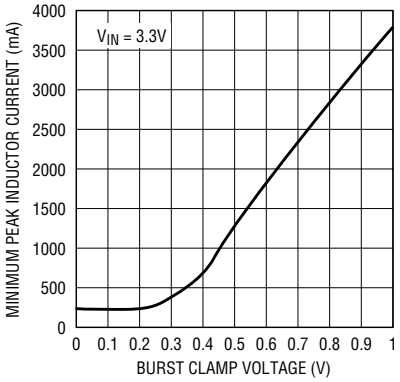

Figure 1. Minimum peak inductor current vs burst clamp voltage

The LTC3412 can be configured for either programmable Burst Mode® operation or Forced Continuous operation. For portable battery-powered applications, Burst Mode operation extends battery life by reducing gate charge losses at light loads—at no load, the LTC3412 consumes a mere 62µA of supply current. Forced Continuous operation, though not as efficient as Burst Mode operation at light loads, maintains a steady operating frequency, making it easier to reduce noise and RF interference—important for some applications.

The LTC3412 provides for external control of the burst clamp level, in effect allowing the burst frequency to be varied. Lower Burst Mode operating frequencies result in improved light load efficiencies, but there is a trade-off between light load efficiency and output voltage ripple—as the Burst Mode frequency decreases, the output ripple increases slightly.

In the LTC3412, the burst clamp level is adjusted by varying the DC voltage at the Sync/Mode pin within

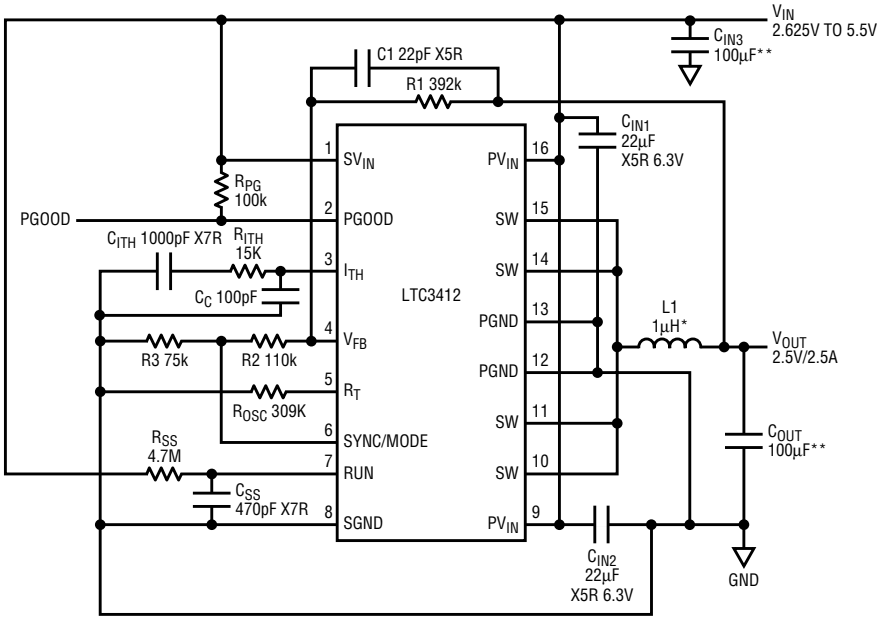

Figure 2. 2.5V, 2.5A regulator using all ceramic capacitors

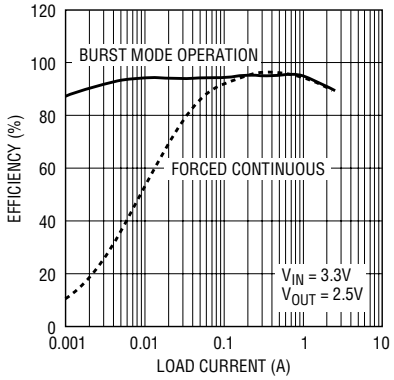

Figure 3. Efficiency vs load current

a 0V–1V range. The voltage level at this pin sets the minimum peak inductor current during each switching cycle in Burst Mode operation. If the minimum peak inductor current delivers more energy than is demanded by the load current, the internal power switches operate intermittently to maintain regulation.

Figure 1 shows the relationship in Burst Mode operation between the minimum peak inductor current during each switching cycle, and the voltage at the Sync/Mode pin. If the minimum peak inductor current is increased, more energy is delivered to the load during each switching cycle. This forces the control loop to skip more cycles, thus lowering the burst frequency required to maintain regulation. This yields greater efficiency, but also slightly increases output ripple. Conversely, lowering the minimum peak inductor current results in less energy delivered to the load during each switching cycle. This forces the control loop to skip fewer cycles, thus increasing the burst frequency, and reducing the output voltage ripple.

Burst Mode operation provides an efficient solution for light-load applications, but sometimes noise suppression takes priority over efficiency. To reduce noise and RF interference, the LTC3412 can be configured for Forced Continuous operation. In this mode, a constant switching frequency is maintained regardless of the output load. This is important for noise sensitive applications in which it is necessary to avoid switching harmonics in a particular signal band. During dropout, the internal P-channel power MOSFET is turned on continuously to extend the useful operating voltage over the life of the battery. As the battery voltage decreases toward the output voltage, the duty cycle and the on-time increase. Further reduction in the battery voltage forces the P-channel power MOSFET to remain on for more than one cycle, that is, raise the duty cycle to 100%.

A High Efficiency 2.5V/2.5A Step-Down Regulator with All Ceramic Capacitors

Figure 2 shows a 2.5V step-down DC/DC converter using all ceramic capacitors. This circuit provides a regulated 2.5V output at up to 2.5A from a 2.625V to 5.5V input. Efficiency for this circuit is as high as 95% for a 3.3V input, as shown in Figure 3.

Ceramic capacitors offer low cost and low ESR, but many switching regulators have difficulty operating with them. The LTC3412, however, includes OPTI-LOOP compensation, which allows it to operate properly with ceramic input and output capacitors.

The problem many switching regulators have when using ceramic capacitors is that their ESR is too low, which leads to loop instability. That is, the phase margin of the control loop can drop to inadequate levels without the aid of the zero that is normally generated from the higher ESR of tantalum capacitors. The LTC3412 allows loop stability to be achieved over a wide range of loads and output capacitors with proper selection of the compensation components on the I_{TH} pin.

The switching frequency for this circuit is set at 1MHz by a single external resistor, R_{OSC}. Operating at frequencies this high allows the use of a lower valued (and physically smaller) inductor and output capacitor. In this particular application, Burst Mode operation maintains the high efficiency at light loads. During Burst Mode operation, switching cycles are skipped during light loads

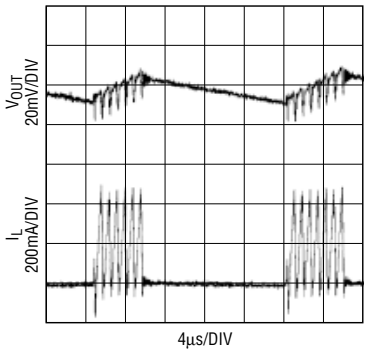

Figure 4. Burst Mode operation

to reduce switching losses. Efficiency is further improved by powering down the majority of the internal circuitry during the intervals between switching cycles. The Burst Mode operation current is set by the R_2 and R_3 voltage divider, which generates a 0.32V reference at the Sync/Mode pin. This corresponds to approximately 450mA minimum peak inductor current, as shown in Figure 1. Figure 4 illustrates how Burst Mode operation produces a burst of inductor current pulses that are repeated periodically. Each inductor current pulse increases to approximately 450mA during each switching period before the main power MOSFET is shut off. The process repeats for a multiple number of switching cycles until the change on the output capacitor is refreshed. Once this is accomplished, both the main and synchronous power MOSFETs are held off while the load current is solely supplied by the charge on the output capacitor. This sleep state continues until the output voltage drops low enough to initiate another burst cycle. Varying the voltage on the Sync/Mode pin affects the amplitude of the group of current bursts as well as the frequency at which they are repeated.

Conclusion

The LTC3412 is a monolithic, synchronous step-down DC/DC converter that is well suited for applications requiring up to 2.5A of output current. Its high switching frequency and internal low $R_{DS(ON)}$ power switches make the LTC3412 an excellent choice for compact, high efficiency power supplies.

White LED Driver in Tiny SC70 Package Achieves 84% Efficiency

by Pit-Leong Wong

Introduction

The LT1937 step-up DC/DC converter is designed to efficiently drive white LED backlights while fitting into tight spaces. The device, available in SC70 and ThinSOT™ packages, provides a conversion efficiency of about 84% when driving 3 LEDs from a Li-Ion cell. The 1.2MHz switching frequency of the LT1937 allows the use of tiny external components. For instance, a 3-LED circuit requires only 0.22µF of output capacitance and only 1µF of input capacitance. An entire LED driver solution can fit into a space under 28mm^2.

Series drive of the LEDs also produces matched light output from each LED independent of the variable LED forward voltage drop, V_F.

The LED current is set at the FB pin of the LT1937. A built-in 95mV reference voltage minimizes power loss in the current-setting resistor, increasing efficiency. Dimming is also easily added with two additional resistors. The input range of 2.5V to 10V, and the internal switch voltage rating of 36V, allow the device to drive two to four LEDs from a Li-Ion cell with plenty of voltage margin.

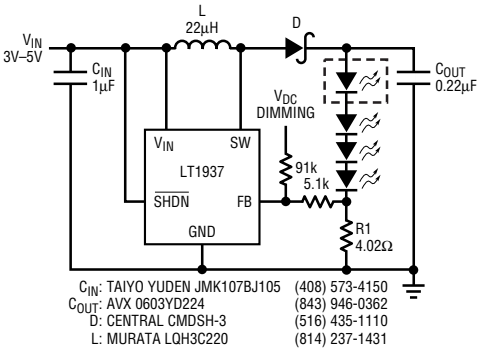

Figure 1. Li-Ion driver for three or four white LEDs

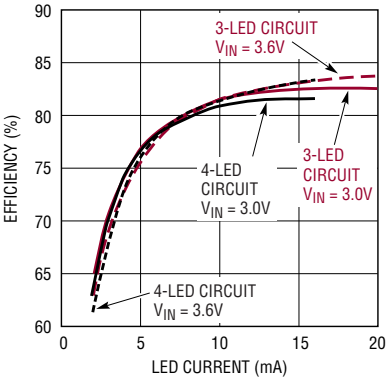

Figure 2. Efficiency of the circuit in Figure 1

Li-Ion Driver for Three or Four White LEDs

The most common application for the LT1937 is to drive three or four white LEDs from a single Li-Ion cell. The circuit and the efficiency curve for three and four white LEDs are shown in Figure 1 and Figure 2, respectively. The efficiencies remain above 80% for most of the LED current range. In these particular circuits, dimming is controlled by a DC voltage. Dimming can also be controlled by logic signals and PWM signals. Consult the LT1937 data sheet for more about LED dimming control. Figure 1 shows just how simple it is to create a complete LED driver solution with the LT1937 and a few external components.

Soft-Start Circuit

To minimize startup delay, no internal soft-startup circuit is included in the LT1937, but it can be implemented with just a few additional external components. Figure 3 shows the components needed for a soft-start LED driver that minimizes the startup inrush current. The switching waveforms in Figure 4 show the limited inrush current during startup.

Conclusion

The LT1937 provides constant current for LEDs, at efficiencies up to 84%, in an extremely compact and easy to use package.

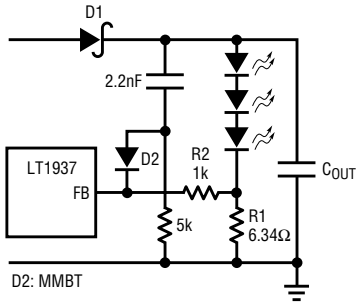

Figure 3. External soft-start circuit

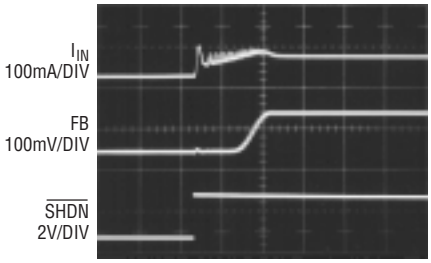

Figure 4. Soft-start waveforms

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Boost DC/DC Converter Synchronizes to any Frequency

by Gary Shockey

Power supplies that employ switching regulators often require tight control over the oscillator switching frequency, mainly in an effort to control high frequency noise that can interfere with sensitive circuitry. The LT1310 switching regulator can be synchronized to an external frequency, thus containing noise to well-defined frequency bands, which can be easily filtered.

The LT1310 combines a 1.5A Boost PWM DC/DC converter with an integrated phase-locked loop, which can be synchronized to any frequency between 10kHz and 4.5MHz. Figure 1 shows an application that converts 5V to 12V with an externally controlled switching frequency of 1.6MHz. To synchronize to an external input signal, the timing capacitor and PLL filter components must be chosen properly. This is a simple process and can be done using the graph in Figure 2.

In Figure 2, operating frequency is plotted versus timing capacitor (C_T) with the upper and lower lines corresponding to the minimum and maximum lock frequency given a specific C_T value. To choose the right timing capacitor, find the intersection of the desired operating frequency and the dashed line. Then move to the corresponding C_T value.

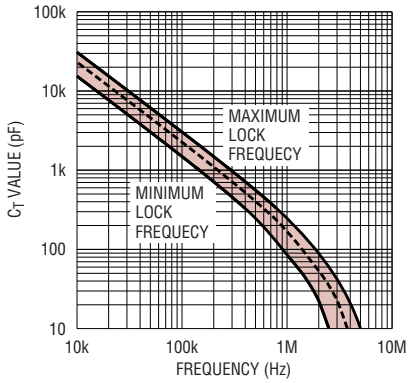
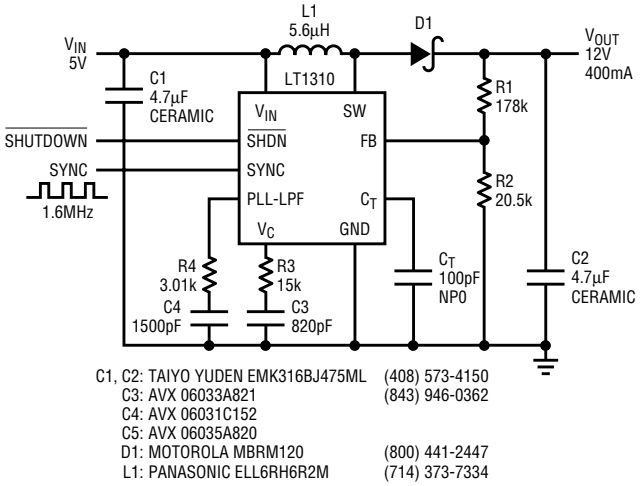


Figure 2. C_T vs operating frequency



C1, C2: TAIYO YUDEN EMK316BJ475ML (408) 573-4150
C3: AVX 06033A821 (843) 946-0362
C4: AVX 06031C152
C5: AVX 06035A820
D1: MOTOROLA MBRM120 (800) 441-2447
L1: PANASONIC ELL6RH6R2M (714) 373-7334

Figure 1. 5V to 12V converter synchronized at 1.6MHz

Alternately, use the following equations as a starting point:

for $f_{LOCK} \geq 2MHz$:

$$C_T = 0.75\left[\frac{250\times10^{-6}}{f_{LOCK}} - 40\times10^{-12}\right]$$

for $f_{LOCK} \leq 2MHz$:

$$C_T = 0.75\left[\frac{310\times10^{-6}}{f_{LOCK}} - 60\times10^{-12}\right]$$

Because the lock range for the PLL is nearly 2:1, the nearest standard value NP0 capacitor can be used. For the application shown in Figure 1, a 1.6MHz switching frequency corresponds to an 100pF timing capacitor. Figure 3 shows the input frequency being stepped from 1.2MHz to 1.9MHz with the PLL regaining lock in approximately 50µs. Since the switching frequency affects inductor ripple current, the inductor must also be scaled. Table 1 shows recommended component values for various switching frequencies.

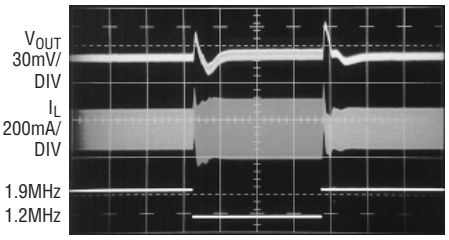


Figure 3. Phase-locked loop response

Table 1: Recommended component values for various switching frequencies (R4 = 3.01k)

Switching Frequency	C_T	C3	C4	R3	L1
600kHz	330pF	1500pF	2700pF	10k	10µH
1MHz	180pF	1000pF	2200pF	10k	6.2µH
1.6MHz	100pF	820pF	1500pF	15k	5.6µH
2MHz	68pF	820pF	1500pF	15k	4.7µH
2.5MHz	47pF	330pF	1500pF	20k	3.3µH
3MHz	33pF	330pF	1000pF	20k	2.7µH

Monolithic Synchronous Step-Down Regulators Pack 600mA Current Rating in a ThinSOT Package

by Jaime Tseng

Introduction

The new LTC®3406, LTC3406-1.5, LTC3406-1.8, LTC3406B, LTC3406B-1.5 and LTC3406B-1.8 are the industry's first monolithic synchronous step-down regulators capable of supplying 600mA of output current in a 1mm profile ThinSOT package. These devices are designed to save space and increase efficiency for battery-powered portable devices. The LTC3406 series uses Burst Mode operation to increase efficiency at light loads, consuming only 20µA of supply current at no load. For noise-sensitive applications, the LTC3406B series disables Burst Mode operation and operates in pulse skipping mode under light loads. Both consume less than 1µA quiescent current in shutdown.

Space Saving

Everything about the LTC3406/LTC3406B series is designed to make power supplies tiny and efficient. An entire regulator can fit into a 5mm×7mm board space. These devices are high efficiency monolithic synchronous buck regulators using a constant frequency, current mode architecture. Their on-chip power MOSFETs provide up to 600mA of continuous output current. Their internal synchronous switches increase efficiency and eliminate the need for an external Schottky diode. Internal loop compensation eliminates additional external components.

Versatile

These devices have a versatile 2.5V to 5.5V input voltage range, which makes them ideal for single cell Li-Ion or 3-cell NiCd and NiMH applications. The 100% duty cycle capability for low dropout allows maximum energy to be extracted from the battery. In dropout, the output voltage is determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor resistance. The fixed voltage output versions—available for 1.5V and 1.8V—require no external voltage divider for feedback, further saving space and improving efficiency. The adjustable voltage output versions—the LTC3406 and LTC3406B—allow the output voltage to be externally programmed with two resistors to any value above the 0.6V internal reference voltage.

Fault Protection

The LTC3406 and LTC3406B protect against output overvoltage, output short-circuit and power overdissipation conditions. When an overvoltage condition at the output (>6.25% above nominal) is sensed, the top MOSFET is turned off until the fault is removed. When the output is shorted to ground, the frequency of the oscillator slows to 210kHz to prevent inductor-current runaway. The frequency returns to 1.5MHz when V_{FB} is allowed to rise to 0.6V. When there is a power overdissipation condition and the junction temperature reaches approximately 160°C, the thermal protection circuit turns off the power MOSFETs allowing the part to cool. Normal operation resumes when the temperature drops to 150°C.

Efficient Burst Mode Operation (LTC3406 Series)

In Burst Mode operation, the internal power MOSFETs operate intermittently based on load demand. Short burst cycles of normal switching are followed by longer idle periods where the load current is supplied by the output capacitor. During the idle period, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 19µA. At no load, the output capacitor discharges slowly through the feedback resistors resulting in very low frequency burst cycles that add only a few microamperes to the supply current.

Pulse Skipping Mode (LTC3406B Series) for Low Noise

Pulse skipping mode lowers output ripple, thus reducing possible interference with audio circuitry. In pulse skipping mode, constant-frequency operation is maintained at lower load currents to lower the output voltage ripple. If the load current is low enough, cycle skipping eventually

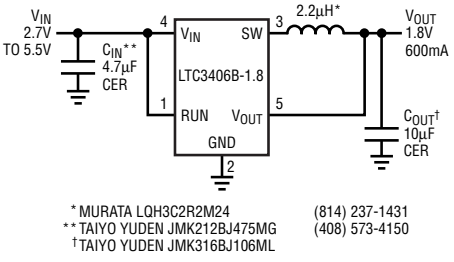


Figure 1. 1.8V/600mA step-down regulator using all ceramic capacitors

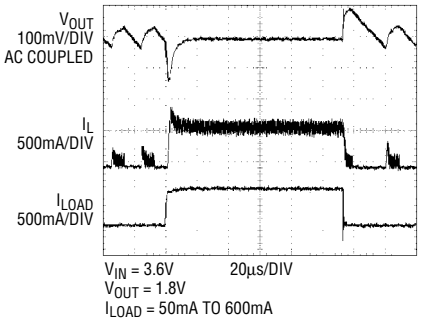


Figure 2. LTC3406-1.8 transient response to a 50mA to 600mA load step

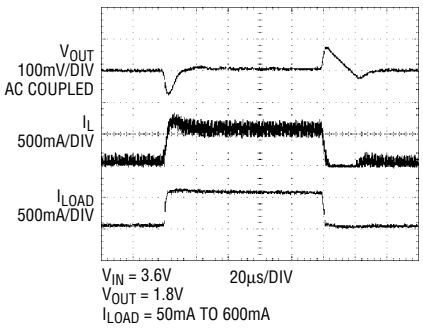


Figure 3. LTC3406B-1.8 Transient Response to a 50mA to 600mA Load Step

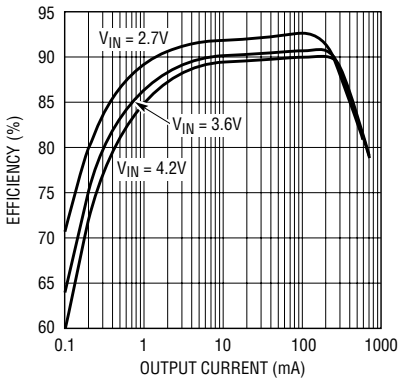


Figure 4. Efficiency vs Load Current for LTC3406-1.8

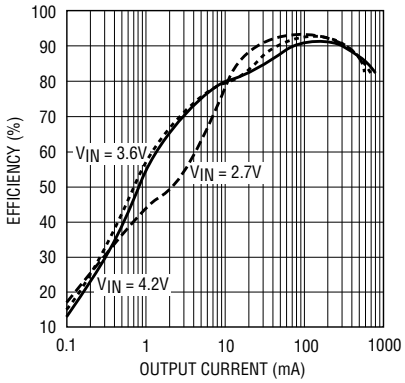


Figure 5. Efficiency vs Load Current for LTC3406B-1.8

occurs to maintain regulation. Efficiency in pulse skipping mode is lower than Burst Mode operation at light loads, but comparable to Burst Mode operation when the output load exceeds 50mA.

1.8V/600mA Step-Down Regulator Using All Ceramic Capacitors

Figure 1 shows an application of the LTC3406/LTC3406B-1.8 using all ceramic capacitors. This particular design supplies a 600mA load at 1.8V with an input supply between 2.5V and 5.5V. Ceramic capacitors have the advantages of small size and low equivalent series resistance (ESR), making possible for very low ripple voltages at both the input and output. For a given package size or capacitance value, ceramic capacitors have lower ESR than other bulk, low ESR capacitor types (including tantalum capacitors, aluminum and organic electrolytics). Because the LTC3406/LTC3406B's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size. Figures 2 and 3 show the transient response to a 50mA to 600mA load step for the LTC3406-1.8 and LTC3406B-1.8, respectively.

Authors can be contacted at (408) 432-1900

Efficiency Considerations

Figure 4 shows the efficiency curves for the LTC3406-1.8 (Burst Mode operation enabled) at various supply voltages. Burst Mode operation significantly lowers the quiescent current, resulting in high efficiencies even with extremely light loads.

Figure 5 shows the efficiency curves for the LTC3406B-1.8 (pulse skipping mode enabled) at various supply voltages. Pulse skipping mode maintains constant-frequency operation at lower load currents. This necessarily increases the gate charge losses and switching losses, which impact efficiency at light loads. Efficiency is still comparable to Burst Mode operation at higher loads.

LTC3720, continued from page 20

optional short-circuit latch-off, a Power Good indicator of output regulation and a current limit foldback for overload protection. A selectable discontinuous conduction mode of operation maintains high efficiency at light loads, when the CPU is running at deep sleep mode, for example, thereby improving battery life in portable applications.

Figure 1 shows the schematic diagram of a 20A VRM8.5 design for an Intel processor operating at 1.2GHz. Efficiency is greater than 80% over a wide load range, as shown in Figure 2. With two 680µF Sanyo POSCAPs, the output voltage deviation remains within the VRM8.5 specification when load current switches between CPU leakage and full load, as shown in Figure 3. The entire VRM design fits into a 1.25"×1.5", double-sided PCB area with an overall height below 0.35".

In summary, the LTC3720 is an ideal device for low current CPU power supplies. Its unique control architecture and its powerful gate drivers facilitate the design of space-saving VRMs that have a fast transient response. For CPUs that consume more than 20A, the LTC1709-85 dual-phase controller addresses the current distribution and thermal management issues associated with higher current applications.

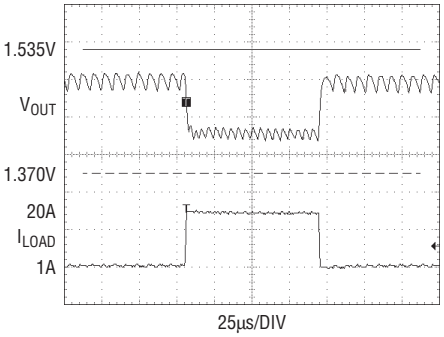


Figure 3. With two POSCAPs at output, the design in Figure 1 meets VRM 8.5 transient requirements with significant margin.

Inductorless, Low Noise Step-Down DC/DC Converter Saves Space and Provides Efficient 1.5V Output

by Bill Walter

Introduction

Linear Technology's new LTC3250-1.5 switched capacitor step-down DC/DC converter squeezes into the tightest spaces while providing up to 250mA of output current at 1.5V from a single 3.1V to 5.5V supply. To keep the converter footprint small, the LTC3250 operates at high frequency, allowing the use of tiny low cost ceramic capacitors—no inductors are required. The LTC3250 is available in a tiny 6-pin ThinSOT package making it possible to build a complete converter in an area of less than 0.04in^2, as shown on the board in Figure 1.

The LTC3250 uses a 2-to-1 switched capacitor fractional conversion mode to achieve a 50% efficiency improvement over that of a linear regulator. A single input and output capacitor, and an external flying capacitor are all that is needed for operation.

The LTC3250 also features Burst Mode operation, which allows the LTC3250 to achieve high efficiency even at light loads. An output current sense circuit is used to detect when the required output current drops below about 30mA. When this occurs, LTC3250 delivers a minimum amount of charge for one cycle then goes into a low current state until the output drops enough to require an-

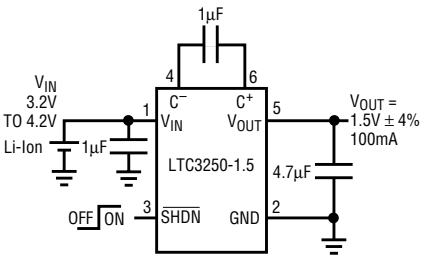


Figure 2. Schematic of the Li-Ion to 1.5V converter shown in Figure 1

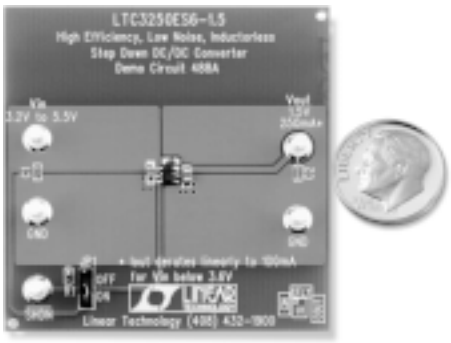


Figure 1. The LTC3250 is available in a tiny 6-pin ThinSOT package making it possible to fit a complete converter in less than 0.04in^2.

other burst of charge. This bursting on and off of the charge pump persists until the load current rises above 30mA at which point constant frequency operation resumes. During Burst Mode operation the current transferred to the output is limited by internal circuitry, thus providing a nearly fixed output ripple of about 10mV$_{P-P}$.

The LTC3250's constant frequency architecture not only provides a low noise regulated output, but also has lower input noise than conventional switched capacitor charge pump regulators. Regulation is achieved by sensing the output voltage and regulating the amount of charge transferred per cycle. This method of regulation provides much lower input and output ripple than that of conventional switched capacitor charge pumps. Charge transfer in the LTC3250 occurs at a constant 1.5MHz frequency making it easy to filter input and output noise. Conventional switched capacitor charge pumps, such as those that use only a Burst Mode architecture to regulate, are much more difficult to filter because they operate over a range of frequencies that can cover several orders of magnitude.

The LTC3250 has built-in short-circuit current limiting as well as over temperature protection. During a short-circuit condition the part automatically limits the output current to approximately 500mA. The LTC3250 shuts down and stops all charge transfer when the IC temperature exceeds approximately 160°C. Under normal operating conditions, the part should not go into thermal shutdown but the function is included to protect the IC from excessively high ambient temperatures, or from excessive power dissipation inside the IC (i.e., overcurrent or short circuit). The charge transfer will reactivate once the junction temperature drops back to approximately 150°C. The LTC3250 can cycle in and out of thermal shutdown indefinitely, without latch-up or damage, until the fault condition is removed.

The $\overline{\text{SHDN}}$ pin is used to implement both low current shutdown and soft-start. Forcing the $\overline{\text{SHDN}}$ pin low puts the LTC3250 into shutdown mode. Shutdown mode disables all control circuitry and forces the output into a high impedance state, leaving only a few nanoamps of supply current. The soft-start feature limits inrush currents required to charge the output capacitor, thereby minimizing input supply transients caused by the power on phase of the IC. The soft-start is implemented whenever the IC is brought out of shutdown.

Conclusion

The LTC3250-1.5 is well suited for medium to low power step-down applications with tight board space and low noise requirements. It is an especially good match for single cell Li-Ion and multicell NiMH/NiCd battery powered applications.

Low Voltage, High Current DC/DC Power Supply with Load Sharing and Redundancy

by Henry J. Zhang and Wei Chen

Introduction

As computer and networking systems get larger and faster, their supply currents continue to rise and their supply voltages continue to drop. Load currents are high enough to require that power supply designers use several power supply modules in parallel. High performance power supplies for data-processing and communication equipment must also provide exceptional reliability and fault tolerance. For example, power systems for mission-critical data processing systems are must be functional better than 99.999% of the time. To satisfy the needs of these systems, the power management solution must provide load sharing, fault tolerance and redundancy.

This article presents a power management solution that offers all of these features in a relatively simple circuit that uses the LTC3729 PolyPhase® controller and LTC4350 hot swappable load-share controller.

About the LTC3729 PolyPhase Controller

The LTC3729 dual current mode PolyPhase controller provides the performance and reliability required by low voltage, high current computer and network systems. The Polyphase technique interleaves the clock signal of several paralleled power stages, thus reducing the input and output ripple current so less capacitance is required. Reduced ripple currents significantly improve the reliability and lifetime of the input and output capacitors. The accurate current sensing scheme of LTC3729 provides additional reliability. Current sharing amongst phases is excellent, making for a uniform thermal distribution, thus ensuring the reliability of power semiconductors and output inductors. Other advanced features of LTC3729 include true remote sensing, integrated high current MOSFET drivers, overvoltage protection, foldback current limit, and optional overcurrent latch-off. All of this adds up to a reliable and high performance low voltage, high current supply.

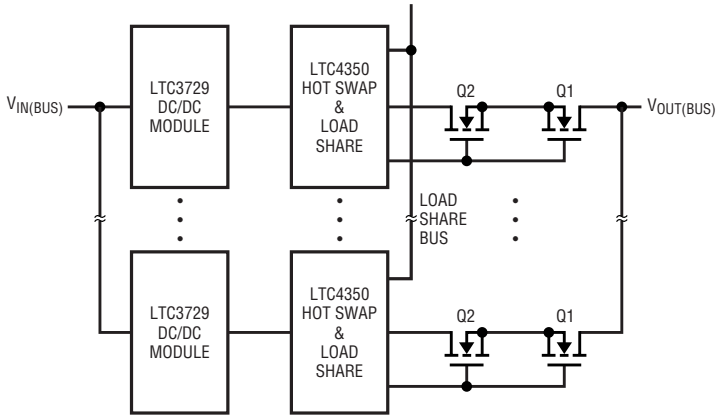


Figure 1. System block diagram of the DC/DC power supplies with load sharing and redundancy

Adding the LTC4350 Hot Swappable Load Share Controller

To further improve system reliability, add the LTC4350 hot swappable load share controller after the LTC3729. The LTC4350 allows paralleled power supplies to share the load with fault tolerance and redundancy. To share the load amongst redundant supplies, the LTC4350 adjusts the output voltage of each supply until the current of each supply matches the value set by the share bus. The LTC4350 also isolates failed supplies by turning off the series output MOSFETs and identifies failed supplies to the system. The failed supply can then be removed and replaced with a new unit without turning off the system power.

The LTC4350 improves system efficiency by allowing the use of low $R_{DS(ON)}$ output MOSFETs instead of ORing diodes.

The LTC4350 is a universal load share controller that works with any DC/DC controller, such as the LTC1628, LTC3728, LTC1629 and LTC1778.

3.3V/40A Output Power Supply with Load Sharing and Redundancy

Figures 2a and 2b show a 3.3V/40A output power supply with load sharing and redundancy. Figure 2a shows the first part of the circuit: the LTC3729 controller in a 2-phase, synchronize buck DC/DC converter that provides 3.3V/40A output from a 5V–12V bus. The converter only requires one IC, eight tiny SO-8 size MOSFETs and two 1µH, low profile, surface mount inductors. Efficiency is 91%–93% over the full input voltage range with a 3.3V/40A output. Figure 3 shows the efficiency of the supply over a wide 2A to 40A load range.

Figure 2b shows the LTC4350 load sharing and hot swap circuit. The load current of each supply is determined by the share bus voltage. For each channel, the I_{OUT} pin of LTC4350 is connected to the voltage feedback

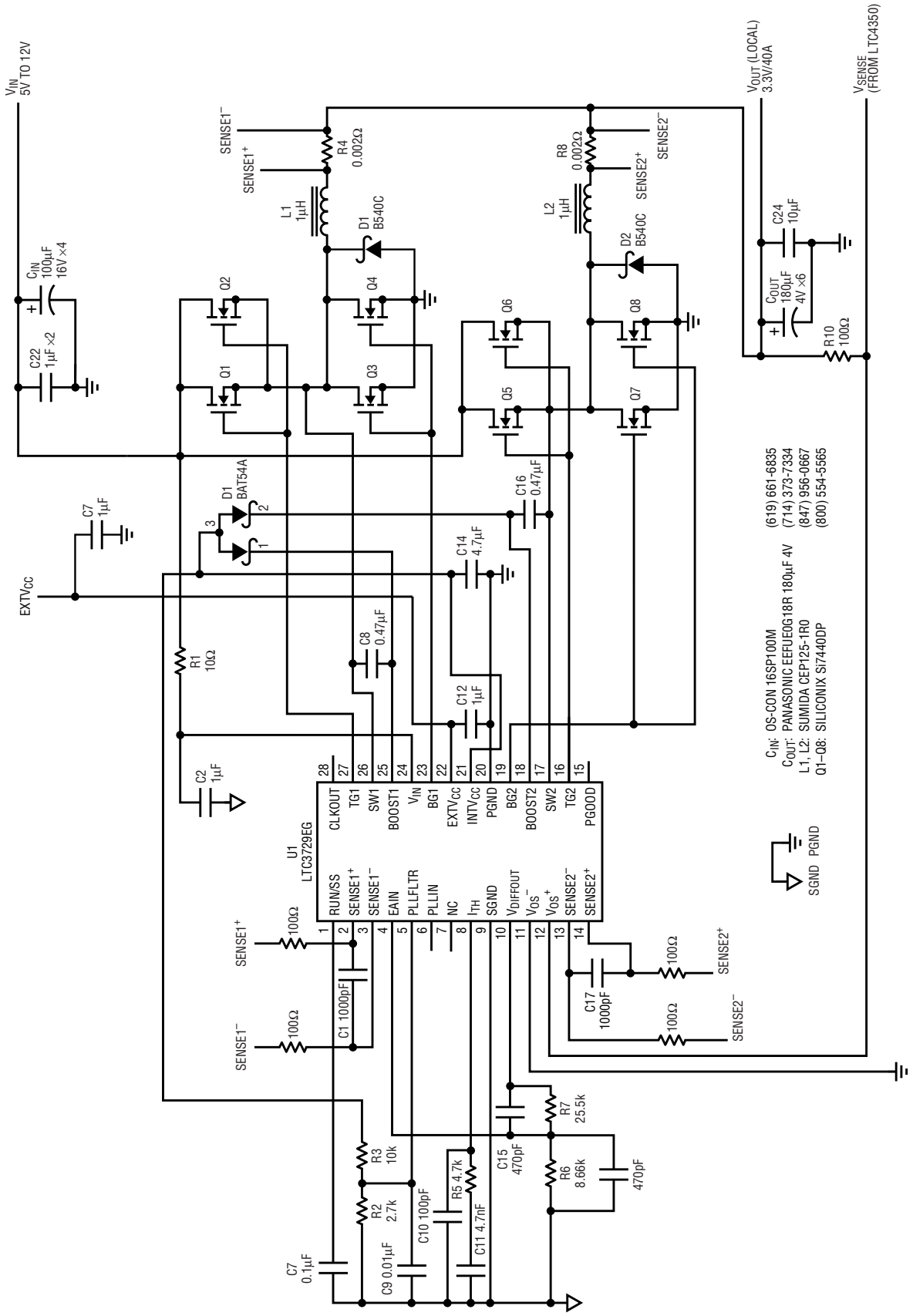


Figure 2a. DC/DC converter portion of the redundant, load sharing power supply

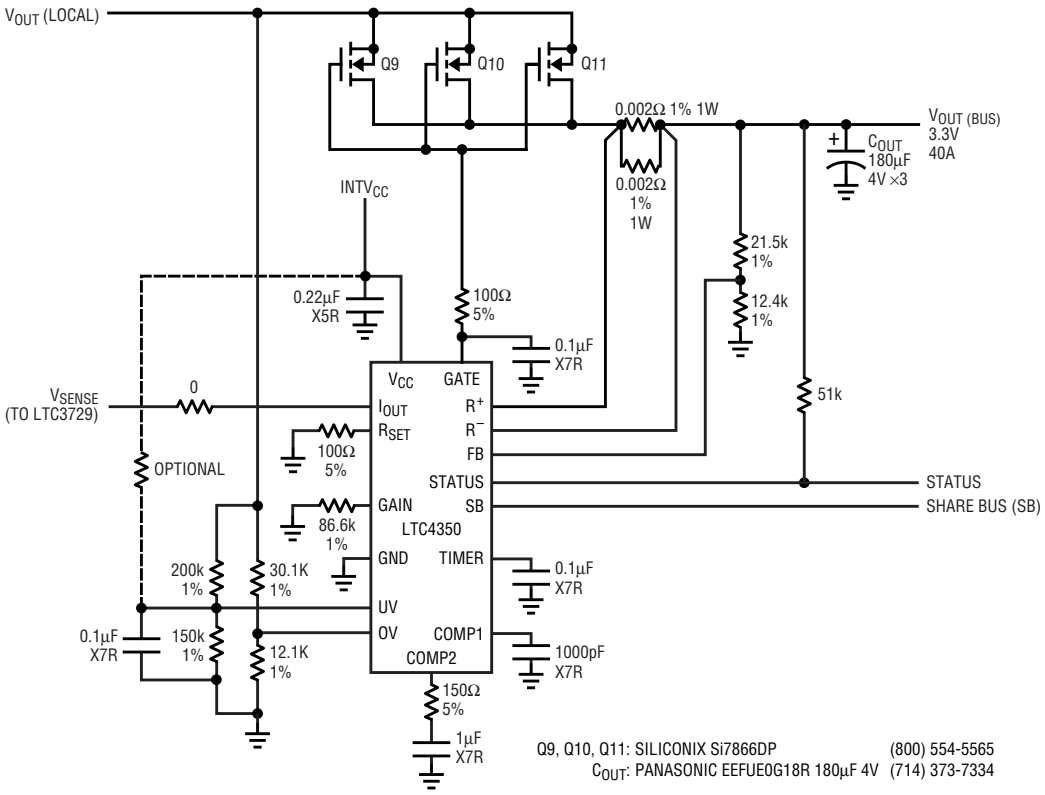


Figure 2b. Load sharing and Hot Swap portion of the power supply solution

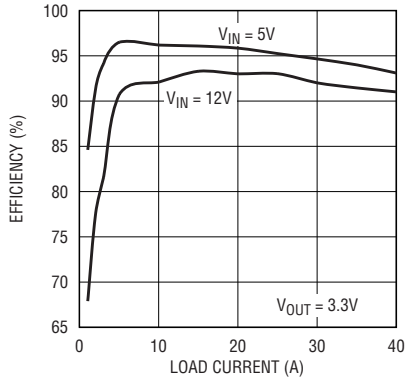


Figure 3. Measured efficiency of the LTC3729 circuit

resistor R10 of the LTC3729. Therefore, the local output voltage V_{OUT} of LTC3729 can be adjusted until the current of each supply matches the value set by the share bus. The LTC4350 monitors the local output voltage V_{OUT} of each supply at the UV (undervoltage) and OV (overvoltage) pins. Low, high and open circuit faults are detected in this way by the LTC4350, which turns off the series output MOSFET to isolate faulty supplies. The LTC4350 also provides an open-drain signal to report the local failure to the system through the STATUS pin. In this design, to simplify the circuit, single-direction MOSFETs are used in each module since the LTC3729 also has output overvoltage and short circuit protection functions.

Figure 4 shows the pulsed load current waveforms of two paralleled power supplies with load sharing. The waveform shows that the two supplies have good current sharing from no load to heavy load, 40A. Figure 5 shows the hot swapping

continued on page 38

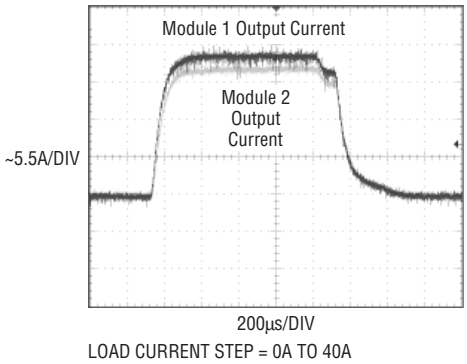


Figure 4. Pulsed load current of two paralleled LTC3729 power supplies with LTC4350

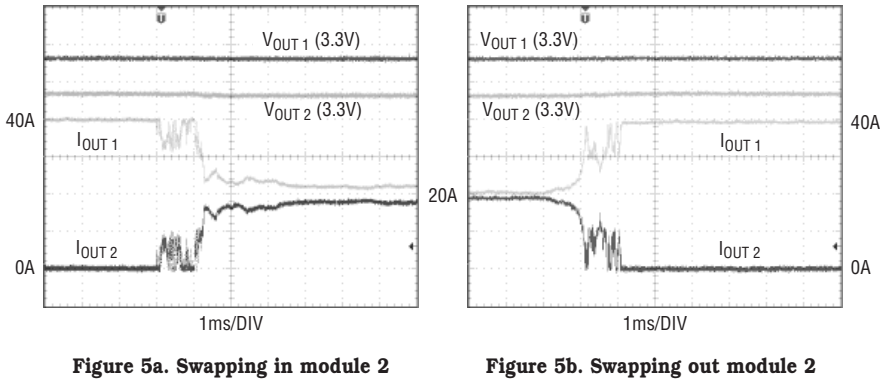


Figure 5a. Swapping in module 2

Figure 5b. Swapping out module 2

Figure 5. Hot swapping waveform of two paralleled LTC3729 supplies with LTC4350

New Device Cameos

Low Power Oscillator Accurately Generates Any Frequency from 1kHz to 20MHz

The LTC6900 is a precision, low power oscillator that is easy to use and occupies very little PC board space. A single external resistor programs the oscillator, capable of generating any frequency from 1kHz to 20MHz (5V supply). The LTC6900 has been designed for high accuracy operation (≤1.5% frequency error) without the need for external trim components. It typically draws only 500µA and features a fast startup time of less than 1.5ms.

The LTC6900 operates with a single 2.7V to 5.5V power supply and provides a rail-to-rail, 50% duty cycle square wave output. The CMOS output driver ensures fast rise/fall times and rail-to-rail switching. The frequency-setting resistor can vary from 10kΩ to 2MΩ to select a master oscillator frequency between 100kHz and 20MHz (5V supply). The three-state DIV input determines whether the master clock is divided by 1, 10 or 100 before driving the output, providing three frequency ranges spanning 1kHz to 20MHz (5V supply). The LTC6900 features a proprietary feedback loop that linearizes the relationship between the external resistor and frequency, eliminating the need for tables to accurately calculate frequency.

The LTC6900 comes in the space-saving low profile (1mm height) ThinSOT-23 package. It is available in both commercial and industrial temperature ranges.

LTC2440: Variable Speed/Resolution 24-Bit ADC Offers Precision and Accuracy from 6.9Hz to 3.5kHz Output Rates

Linear Technology introduces the LTC2440, 24-bit, No Latency Delta-Sigma™ ADC, which uses a patented variable speed/resolution architecture that maintains absolute accuracy independent of the output rate. Ten speed/resolution combinations from 6.9Hz with simultaneous 50/60Hz rejection and 200nV$_{RMS}$ noise, up to 3.5kHz (17 bits) are selectable through an easy to use serial interface. Transparent offset and full-scale calibration ensure stable output codes independent of the speed/resolution selection. A high speed (880Hz output rate), low noise (2µV$_{RMS}$) mode enables users to precisely track rapidly changing input signals. No latency allows users to change speed/resolution or external input channel between conversion cycles without settling errors.

Following each conversion, the device enters a low power auto sleep mode. The duration of the auto sleep state may be extended to reduce the average power dissipation. While running at a 3.5kHz conversion rate, the LTC2440 average current can be reduced to 240µA when reading data at a 100Hz output rate.

An ultralow noise mode eliminates the complexities of PGAs by offering 25 million counts over a ±2.5V input range, or independent of sensor offset/tare voltages, 500,000 counts over a ±50mV input range. The absolute accuracy, independent of output rate (5ppm INL, 1ppm offset, 10ppm full-scale), and flexible input range (common mode input GND to V_{CC} independent of V_{REF}) greatly simplify analog front end circuitry.

LT1819: 400MHz, 2500V/µs Dual Op Amp Slews Fast and Distorts Little

The LT1819 is a low distortion dual op amp with a 400MHz gain bandwidth product and a 2500V/µs slew rate, the fastest of any amplifier from Linear Technology. The part operates with supplies from ±2V to ±6V and draws a typical supply current of only 9mA per amplifier.

The amplifiers can drive 100Ω loads with a low distortion of –85dBc relative to a 5MHz, 2V$_{P-P}$ signal. The output swings to 0.9V from either supply rail with a 500Ω load, and to 1.2V with a 100Ω load. With the outputs at ±3V, the amplifier can sink or source a current of ±80mA.

The low distortion, good output drive capability, and the 6nV/√Hz input voltage noise make the LT1819 an ideal choice for receivers, filters, or drivers of cables and ADCs in high-speed communication or data acquisition systems.

The LT1819 dual op amp is available in an 8-lead SO package. The part is fully specified at ±5V and single 5V supplies, and is available in commercial and industrial temperature grades.

LT1961, High Current, High Frequency Monolithic Boost Converter in a Small MSOP-8 Package Allows Compact PC Board Layouts

The LT1961 is a 1.25MHz, 1.5A maximum switch current, current mode, monolithic boost converter. Packaged in a fused lead frame MSOP-8, it allows very compact PC board layout. High frequency operation enables the use of small external components, including ceramic capacitors, throughout the design. It can be operated in all standard configurations including boost, flyback, forward, inverting, and "Cuk." Included in the

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

MSOP-8 packaged LT1961 are a high efficiency 1.5A switch and all the control circuitry required for a complete current mode buck converter. A patented anti-slope circuit maintains the 1.5A maximum switch current limit over all duty cycles.

Low switch resistance maintains high efficiency at a high switching frequency over the 35V maximum switch voltage range. A low dropout internal regulator ensures consistent performance over the part's entire 2.7V to 30V input range. The accurate shutdown threshold, which reduces quiescent current to 6µA, can be used as a precise undervoltage lockout. Synchronization allows an external logic level signal to increase the internal oscillator frequency from 1.4MHz to 2MHz.

LT6550 and LT6551: 3.3V Triple and Quad Video Amplifiers

The LT6550 and LT6551 are triple and quad video amplifiers designed to operate from a single 3.3V supply. These voltage feedback amplifiers drive double-terminated 50Ω or 75Ω cables and are configured for a fixed gain of 2, eliminating either six or eight external gain setting resistors. The LT6551 quad is designed for single supply operation and performance is fully specified on single 3.3V and 5V supplies. The LT6550 triple can be used on either single or split supplies of ±5V. The LT6550 and LT6551 both feature 110MHz –3dB bandwidth, 340V/µs slew rate and 3% settling time in 20ns, making them ideal for RGB video processing with a maximum screen resolution of 1024 x 768 on a single 3.3V supply.

On a single 3.3V supply, the input voltage range extends from ground to 1.55V and the output swings to within 400mV of the supply voltage while driving a 150Ω load. These features, combined with the ability to accept RGB video signals without the need for AC coupling or level shifting of the incoming signals, make the LT6550 and LT6551 ideal choices for low voltage video applications.

Both the LT6550 and LT6551 are available in a small 10-pin MSOP package and utilize a flow-thru pin out. Each device is available in both commercial and industrial temperature range versions.

LTC3729/LTC4350, continued from page 36

waveforms of two paralleled modules with a total of 40A output current. The settling time for load transients and hot swap load currents can be adjusted via the compensation resistors and capacitors on the COMP1 and COMP2 pins of the LTC4350. See the LTC4350 data sheet for details.

Redundancy for Multiple Output Applications

Figure 6 shows a simple and robust redundant power supply system with three outputs. In this example, three LTC3728 (similar to the LTC3729, but with two outputs) dual output PolyPhase controllers provide voltage control, and six LTC4350s provide hot swappable load sharing. Each LTC3728 regulates two outputs which are switched 180-degrees out of phase to minimize the number of input capacitors.

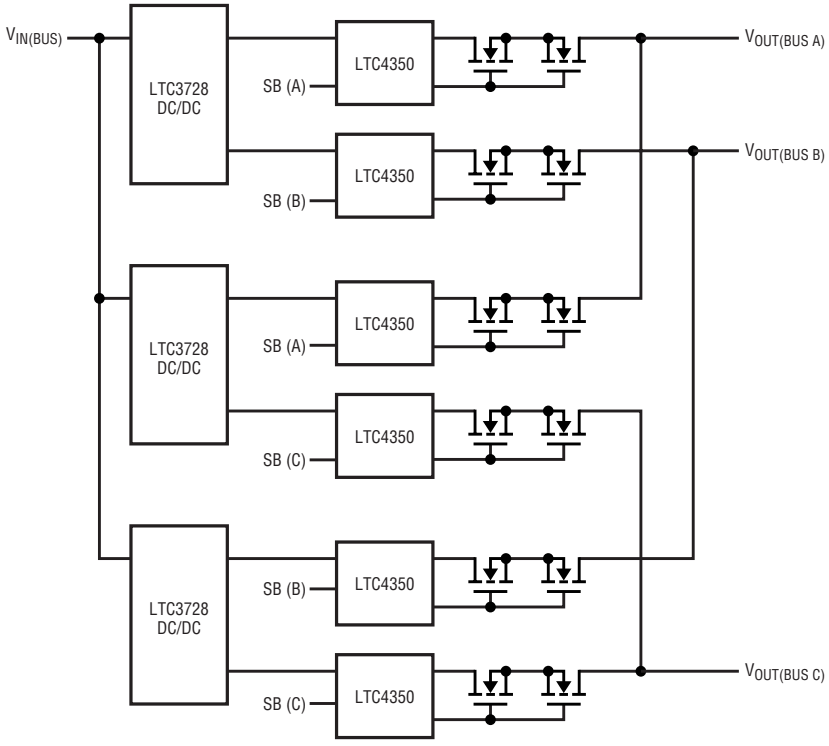


Figure 6. Block diagram of a redundant multiple voltage output system

Conclusion

The LTC3729 PolyPhase current mode controller and dual output LTC3728 provide high performance, minimize component count and increase the reliability of low voltage, high current power supplies. These parts, combined with the LTC4350 hot swappable load share controller, make for easy-to-design fault tolerant redundant power supply systems that are suitable for mission-critical applications.

DESIGN TOOLS

Databooks and Applications Handbooks

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook includes all products introduced in 1991 and 1992. $10.00

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1999 Linear Databook, Vol VII — This 1968 page supplement to the 1990, 1992, 1994, 1995, 1996 and 1997 Linear Databooks includes all products introduced since 1997. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

Brochures and Software

Power Management Solutions Brochure — This 96 page collection of circuits contains real-life solutions for common power supply design problems. There are over 70 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, desktop PC power supplies, notebook PC power supplies, portable electronics power supplies, distributed power supplies, telecommunications and isolated power supplies, off-line power supplies and power management circuits. Selection guides are provided for each section and a variety of helpful design tools are also listed for quick reference. Available at no charge

Data Conversion Solutions Brochure — This 88 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 40 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include delta-sigma ADCs, low power and high speed ADCs and low power and high speed DACs. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included. Available at no charge

Telecommunications Solutions Brochure —This 76 page collection of application circuits and selection guides covers a wide variety of products targeted for telecommunications. Circuits solve real life problems for central office switching, cellular phones, high speed modems, basestation, plus special sections covering –48V and Hot Swap™ applications. Many applications highlight new products such as Hot Swap controllers, power products, high speed amplifiers, A/D converters, interface transceivers and filters. Includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge

SwitcherCAD™ III — LTC SwitcherCAD III is a fully functional SPICE simulator with enhancements and models to ease the simulation of switching regulators. This SPICE is a high performance circuit simulator and integrated waveform viewer, and also includes schematic capture. Our enhancements to SPICE result in much faster simulation of switching regulators than is possible with normal SPICE simulators. SwitcherCAD III includes SPICE, macromodels for 80% of LTC's switching regulators and over 200 op amp models. It also includes models of resistors, transistors and MOSFETs. With this SPICE simulator, most switching regulator waveforms can be viewed in a few minutes on a high performance PC. Circuits using op amps and transistors can also be easily simulated. Download at www.linear.com

FilterCAD™ 3.0 — FilterCAD 3.0 is a computer aided design program for creating filters with Linear Technology's filter ICs. Filter CAD is designed to help users without special expertise in filter design to design good filters with a minimum of effort. It can also help experienced filter designers achieve better results by playing "what if" with the configuration and values of various components and observing the results. With FCAD, you can design lowpass, highpass, bandpass or notch filters with a variety of responses, including Butterworth, Bessel, Chebychev, elliptic and minimum Q elliptic, plus custom responses. Download at www.linear.com

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

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